BAT32G127 Datasheet

Ultra-low power 32-bit microcontrollers based on ARM® Cortex®-M0+

128KB Flash, analog functions, timers and communication interfaces.

V0.1.8

Features

- **Ultra-low power operation environment:**
  - Supply voltage range: 1.8V to 5.5V
  - Temperature range: -40˚C to 105˚C
  - Low power consumption modes: sleep mode, deep sleep mode
  - Operating power consumption: 35uA/MHz@32MHz
  - Power consumption in deep sleep mode: 0.7uA
  - Operation in deep sleep mode +32.768K+RTC: 0.9uA
- **Core:**
  - ARM® 32-bit Cortex®-M0+ CPU
  - Operating frequency: 32KHz to 32MHz
- **Memory:**
  - 128KB Flash memory with shared program and data storage
  - 2.5KB dedicated data Flash memory
  - 8KB SRAM memory with parity check
- **Power and reset management:**
  - Built-in power-on reset (POR) circuit
  - Built-in voltage detection (LVD) circuit (settable threshold voltage)
- **Clock management:**
  - Built-in a high-speed oscillator with accuracy of ±1%, supporting 1MHz to 32MHz system clocks and peripheral module operation clocks
  - Built-in a 32KHz low-speed oscillator
  - Support 1MHz to 20MHz external crystal oscillators
  - Support 32.768KHz external crystal oscillators
- **Multiplier module:**
  - Support 32-cycle 32-bit multiplication operations
- **Enhanced DMA controller:**
  - Interrupt trigger start.
  - Selectable transfer modes (normal transfer mode, repeat transfer mode, block transfer mode and chain transfer mode)
  - Transfer source/destination realm are
- **Rich analog peripherals:**
  - 12-bit ADC converter with a conversion rate of 0.71 Msps. It has 26 external analog channels and selectable internal OPA outputs as conversion channels. It includes a temperature sensor and supports single-channel conversion mode and multi-channel scan conversion mode. Conversion range: 0 to positive reference voltage.
  - Comparator (CMP) with two built-in channels. Input sources are selectable, and reference voltage options include external pin inputs (2), internal reference voltage (1.45V), or outputs from an 8-bit DAC.
  - Operational amplifier (OPA) with a one-channel OPA.
  - 8-bit resolution D/A converter for controlling analog outputs.
- **Input/output ports:**
  - I/O ports: 38 to 60
  - N-channel open drain, internal pull-up and pull-down switching
  - Built-in key interrupt checkout function
  - Control circuit for built-in clock output/buzzer outputs
- **Serial two-wire debugger (SWD)**
- **Rich timers:**
  - 16-bit timer: 8 channels
  - 15-bit interval timer: 1x
  - Real Time Clock (RTC): 1x (with perpetual calendar, alarm function, and support a wide range of clock correction)
  - Watchdog timer (WWDT): 1x
  - SysTick timer
  - Timer A
- **Rich and flexible interfaces:**
  - 3-channel serial communication unit: each channel can be freely configured as a 1-channel standard UART, 2-channel SPI or 2-channel simplified I^2C
  - UART0 supporting LIN-bus receive function
  - Standard SPI: 1 channel (support 8bit and 16bit)
  - Standard I^2C: 1 channel
  - IrDA: 1 channel

selectable from the full address space range

- **Linkage controller:**
  - It can link event signals to realize the linkage of peripheral functions
  - 16 input events and 6 trigger events
- **LCD controller/driver**
  - LCD supports 4COM*42SEG/6COM*40SEG/8COM*38SEG
- **Safety function:**
  - Comply with IEC/UL 60730 standards
  - Report abnormal storage access errors
  - Support RAM parity check
  - Support hardware CRC
  - Support SFR guard and avoid misoperation
  - 128-bit unique ID
  - Flash Level 2 protection in the debug mode (Level1: only perform flash full-scale erase, cannot be read or written. Level2: Emulator connection is invalid, cannot operate on flash.)
- **Package:**
  - 64LQFP, 48LQFP, and 40QFN

1 Overview

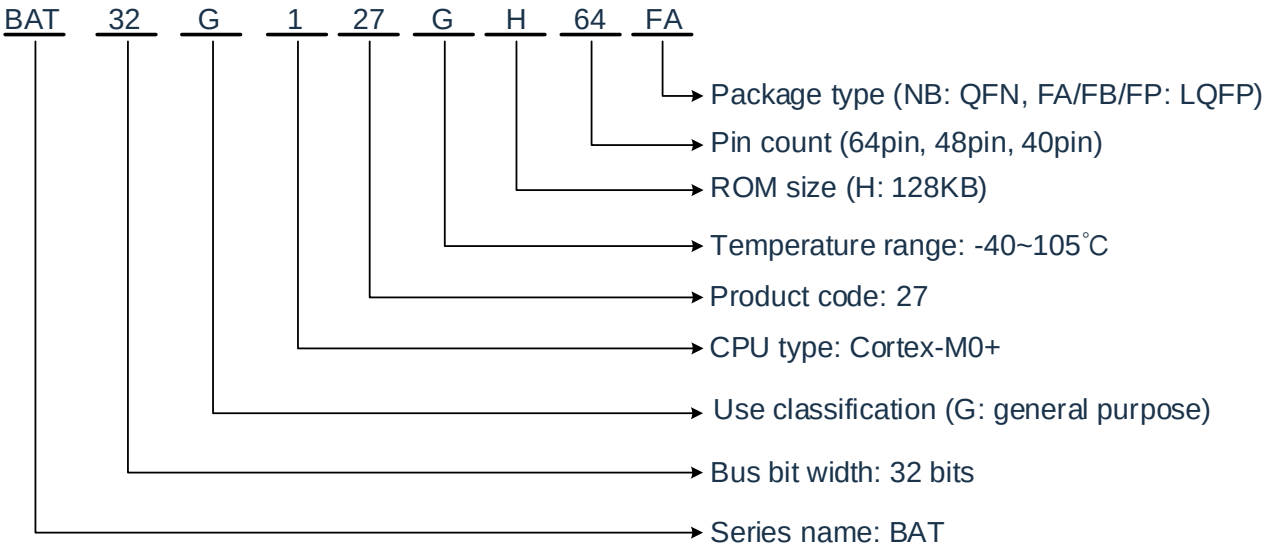
1.1 Brief introduction

The ultra-low-power BAT32G127 features a high-performance ARM®Cortex®-M0+ 32-bit RISC core, capable of operating up to 32 MHz. It includes high-speed embedded flash memory (up to 8KB SRAM and up to 128KB program/data flash). This product integrates multiple standard interfaces such as I2C, SPI, and UART, and supports C-Type/R-Type LCD drivers. It intergrates a 12-bit A/D converter, temperature sensor, comparator, and operational amplifier. The 12-bit A/D converter can be used to capture external sensor signals, reducing system design costs. The integrated temperature sensor allows for real-time monitoring of external environmental temperature. The integrated comparator supports both high-speed and low-speed operating modes. In high-speed mode, it can support feedback control for high-speed motors, while in low-speed mode, it can be used for battery monitoring. The BAT32G127 also features an 8-channel 16-bit timer module, which, in conjunction with the timer, can control a DC motor or two stepper motors.

The BAT32G127 excels in low-power performance, supporting both sleep and deep sleep modes for energy efficiency. Its operating power consumption is 35μA/MHz at 32 MHz, and in deep sleep mode, the consumption is only 0.7μA, making it suitable for battery-powered low-power devices. Additionally, the integration of an event-driven controller allows for direct connections between hardware modules without CPU intervention, providing faster response times compared to interrupt-based systems and reducing CPU activity, thereby extending battery life.

These features make the BAT32G127 microcontroller series suitable for battery-powered LCD display products such as smart water meters, heat meters, gas meters, measurement instruments, and temperature controllers.

1.2 Product model list



BAT32G127 product list:

Pin count	Package	Product model
40 pins	40-pin plastic package QFN (5x5mm, 0.4mm pitch)	BAT32G127GH40NB
48 pins	48-pin plastic package LQFP (7x7mm, 0.5mm pitch)	BAT32G127GH48FA
64 pins	64-pin plastic package LQFP (7x7mm, 0.4mm pitch)	BAT32G127GH64FB

Capacity of FLASH and SRAM:

Flash memory	Dedicated data Flash memory	SRAM	40-pin /48-pin /64-pin
128KB	2.5KB	8KB	BAT32G127

BAT32G127 product list:

Part No.	Core	Clock frequency (MHz)	Min. operating voltage (V)	Max. operating voltage (V)	Code Flash (KB)	SRAM (KB)	Data Flash (KB)	DMA	GPIO	12bit ADC	8bit DAC	CMP	PGA	Universal timer (16bit)	RTC	WDT	UART	SPI	IIC bus	IrDA bus	LIN bus	CAN bus	Hardware multiplier	Hardware divider	Package
BAT32G127 GH40NB	M0+	32	1.8	5.5	128	8	2.5	24	38	16	1	2	1	9	1	1	3	6+1	6+1	1	1	-	Y	Y	QFN 40
BAT32G127 GH48FA	M0+	32	1.8	5.5	128	8	2.5	24	44	17	1	2	1	9	1	1	3	6+1	6+1	1	1	-	Y	Y	LQFP 48
BAT32G127 GH64FB	M0+	32	1.8	5.5	128	8	2.5	24	60	26	1	2	1	9	1	1	3	6+1	6+1	1	1	-	Y	Y	LQFP 64

1.3 Top view

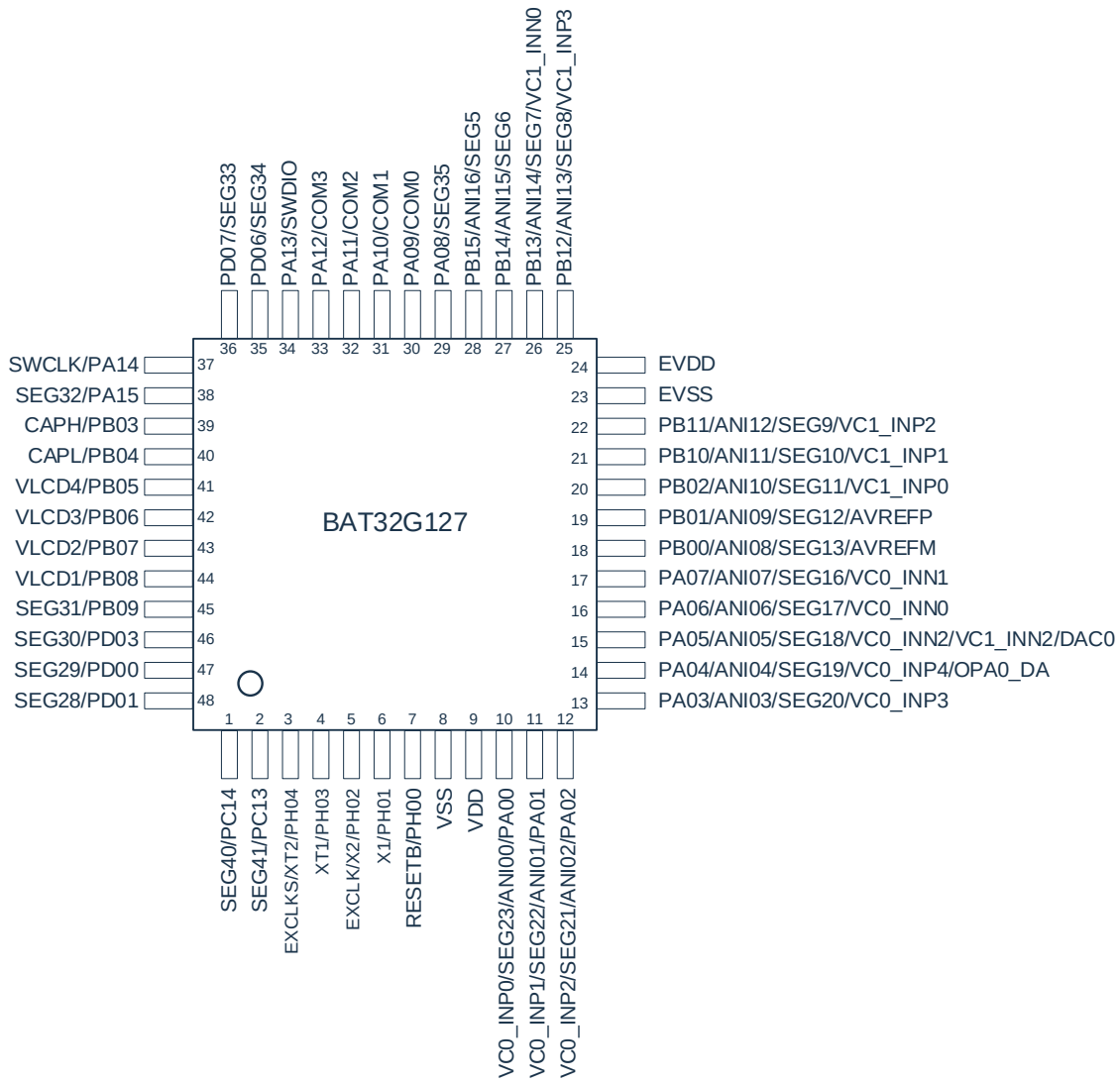
1.3.1 BAT32G127GH40NB

- 40-pin plastic package QFN (5x5mm, 0.4mm pitch)

Note: The functions not labeled in the figure are configurable via pins, see Section 4.1 for details.

1.3.2 BAT32G127GH48FA

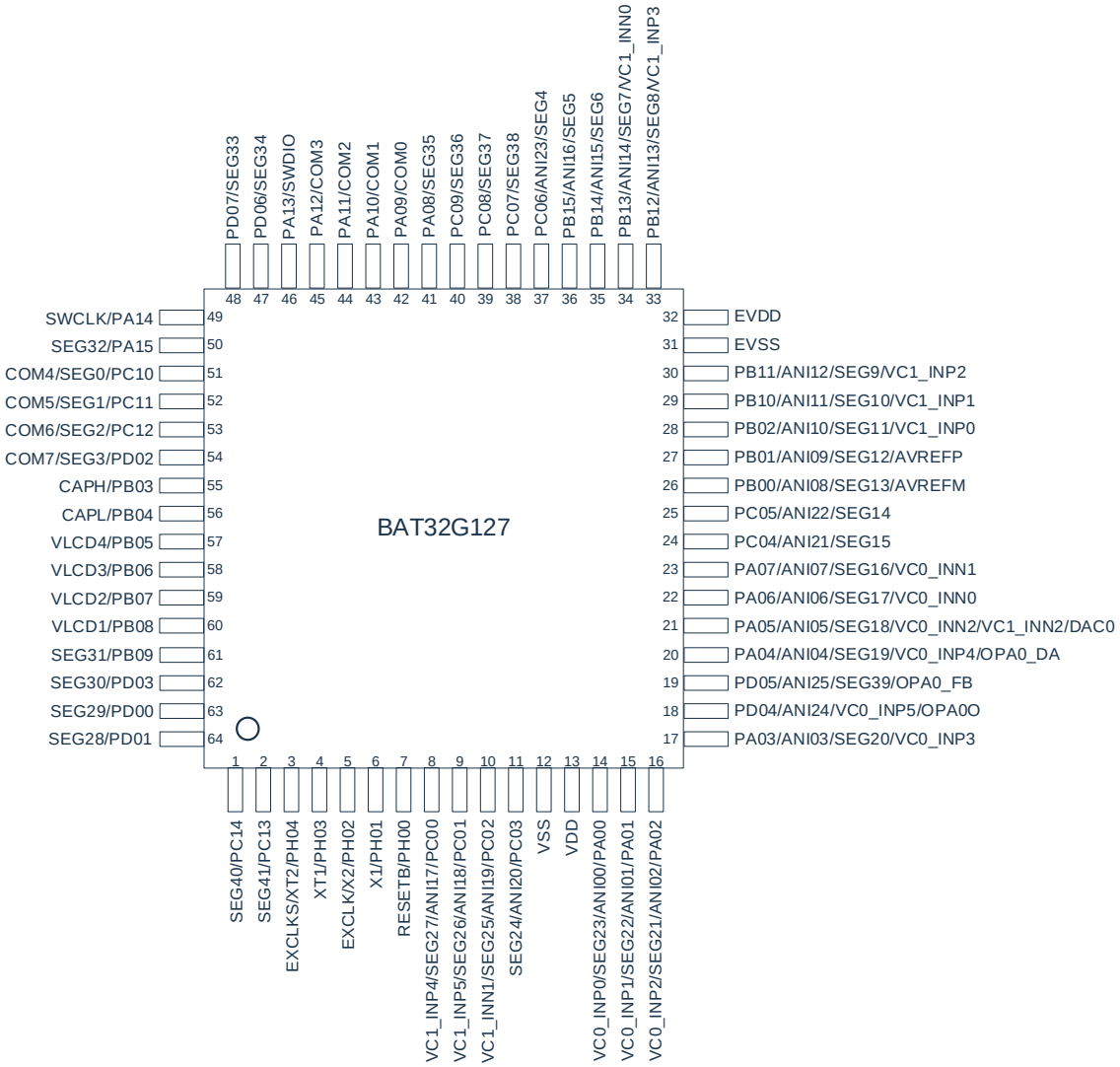
- 48-pin plastic package LQFP (7x7mm, 0.5mm pitch)



Note: The functions not labeled in the figure are configurable via pins, see Section 4.1 for details.

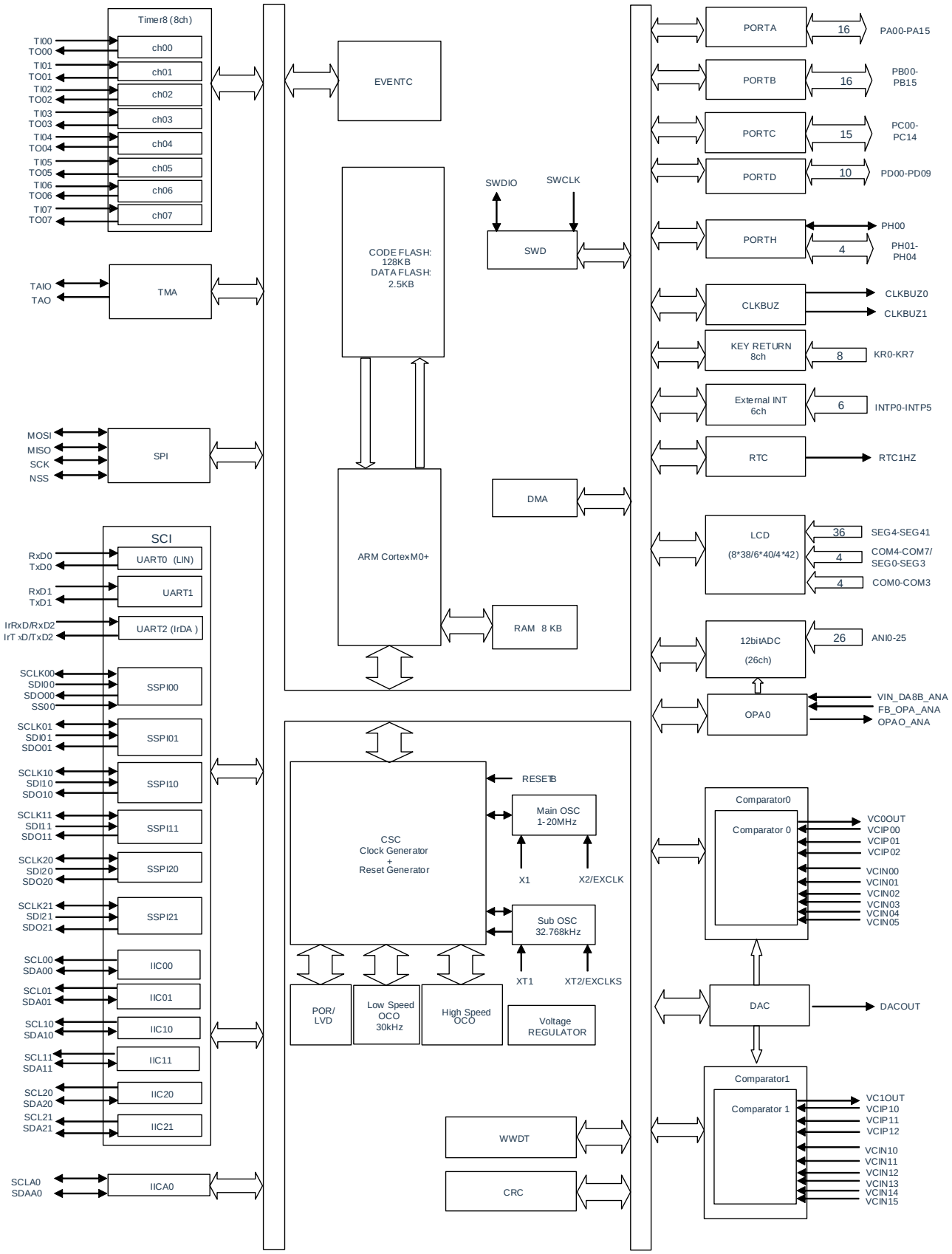
1.3.3 BAT32G127GH64FB

- 64-pin plastic package LQFP (7x7mm, 0.4mm pitch)

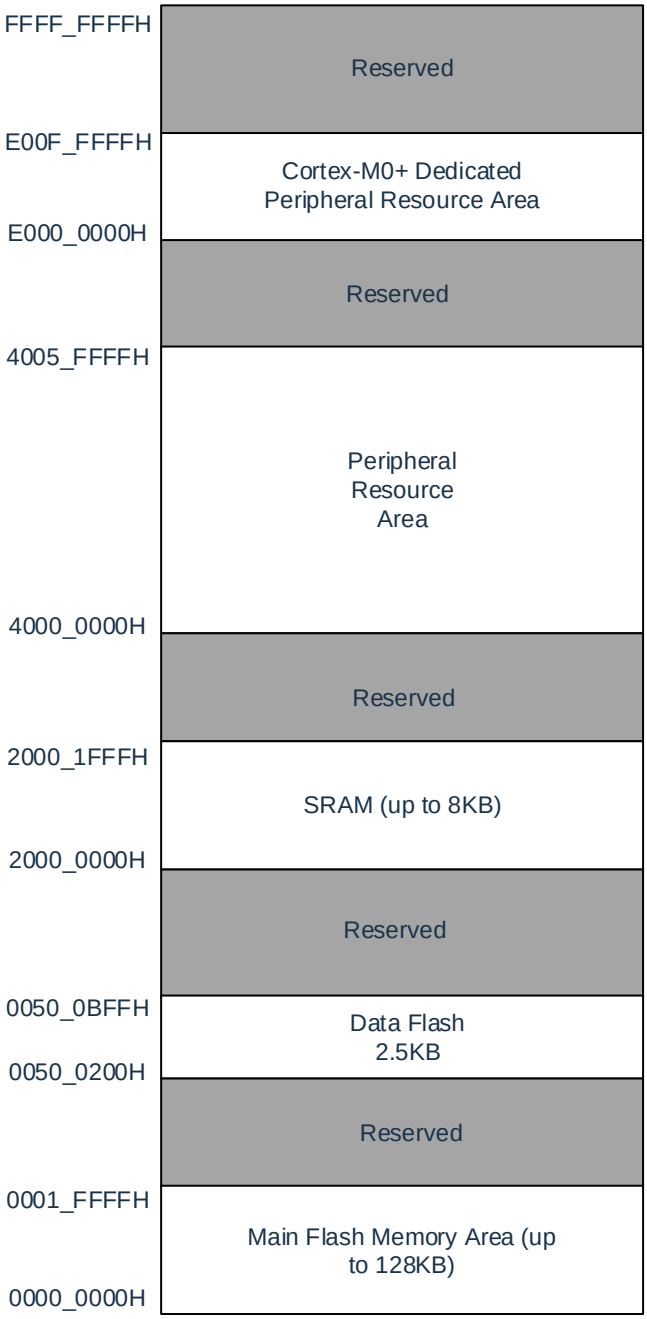


Note: The functions not labeled in the figure are configurable via pins, see Section 4.1 for details.

2 Product Structure Diagram



3 Memory Map


FFFF_FFFFH
Reserved
E00F_FFFFH
Cortex-M0+ Dedicated Peripheral Resource Area
E000_0000H
Reserved
4005_FFFFH
Peripheral Resource Area
4000_0000H
Reserved
2000_1FFFH
SRAM (up to 8KB)
2000_0000H
Reserved
0050_0BFFH
Data Flash 2.5KB
0050_0200H
Reserved
0001_FFFFH
Main Flash Memory Area (up to 128KB)
0000_0000H

4 Pin Functions

4.1 Port function

Table 4.1.1 (1/8)

Port name	Alternate function	Digital output function setting register pxxcfg[2:0]	Function		
			64LQFP	48LQFP	40QFN
PH00	RESETB	RSTM=0 (default function)	●	●	●
	GPIO	RSTM=1	●	●	●
PA00	TXD2/SDO20	3'h01	●	●	-
	TI00	3'h02	●	●	-
	TO00	3'h03	●	●	-
	VC0OUT	3'h06	●	●	-
	GPIO	3'h00	●	●	-
PA01	RXD2/SDI20/SDA20	3'h01	●	●	●
	TI01/TO01	3'h03	●	●	●
	SPI0_MOSI	3'h05	●	●	●
	PCLBUZ0	3'h07	●	●	●
	GPIO	3'h00	●	●	●
PA02	TXD1/SDO10	3'h01	●	●	●
	TI02/TO02	3'h03	●	●	●
	SPI0_MISO	3'h05	●	●	●
	VC1OUT	3'h06	●	●	●
	PCLBUZ1	3'h07	●	●	●
	GPIO	3'h00	●	●	●
PA03	RXD1/SDI10/SDA10	3'h01	●	●	●
	TI03/TO03	3'h03	●	●	●
	TI00_GATE	3'h04	●	●	●
	SPI0_NSS	3'h05	●	●	●
	GPIO	3'h00	●	●	●
PA04	TXD1/SDO10	3'h01	●	●	●
	TI04/TO04	3'h03	●	●	●
	SPI0_NSS	3'h05	●	●	●
	GPIO	3'h00	●	●	●

Table 4.1.1 (2/8)

Port name	Alternate function	Digital output function setting register pxxcfg[2:0]	Function		
			64LQFP	48LQFP	40QFN
PA05	SS10	3'h01	●	●	●
	TI05/TO05	3'h03	●	●	●
	TI06_GATE	3'h04	●	●	●
	SPI0_SCK	3'h05	●	●	●
	PCLBUZ0	3'h07	●	●	●
	GPIO	3'h00	●	●	●
PA06	SS20	3'h01	●	●	●
	TI06/TO06	3'h03	●	●	●
	TI07_GATE	3'h04	●	●	●
	SPI0_MISO	3'h05	●	●	●
	VC0OUT	3'h06	●	●	●
	GPIO	3'h00	●	●	●
PA07	SCLK10/SCL10	3'h01	●	●	●
	TI07/TO07	3'h03	●	●	●
	SPI0_MOSI	3'h05	●	●	●
	VC1OUT	3'h06	●	●	●
	PCLBUZ1	3'h07	●	●	●
	GPIO	3'h00	●	●	●
PA08	TXD0/SDO00	3'h01	●	●	●
	TI00	3'h02	●	●	●
	TO00	3'h03	●	●	●
	TI01_GATE	3'h04	●	●	●
	GPIO	3'h00	●	●	●
PA09	TXD0/SDO00	3'h01	●	●	●
	SCLA0	3'h02	●	●	●
	TI01/TO01	3'h03	●	●	●
	TI02_GATE	3'h04	●	●	●
	PCLBUZ0	3'h07	●	●	●
	GPIO	3'h00	●	●	●
PA10	RXD0/SDI00/SDA00	3'h01	●	●	●
	SDAA0	3'h02	●	●	●
	TI02/TO02	3'h03	●	●	●
	TI03_GATE	3'h04	●	●	●
	PCLBUZ1	3'h07	●	●	●
	GPIO	3'h00	●	●	●

Table 4.1.1 (3/8)

Port name	Alternate function	Digital output function setting register pxxcfg[2:0]	Function		
			64LQFP	48LQFP	40QFN
PA11	SS00	3'h01	●	●	●
	SCLA0	3'h02	●	●	●
	TI03/TO03	3'h03	●	●	●
	TI04_GATE	3'h04	●	●	●
	SPI0_MISO	3'h05	●	●	●
	VC0OUT	3'h06	●	●	●
	GPIO	3'h00	●	●	●
PA12	SS11	3'h01	●	●	●
	SDAA0	3'h02	●	●	●
	TI04/TO04	3'h03	●	●	●
	TI05_GATE	3'h04	●	●	●
	SPI0_MOSI	3'h05	●	●	●
	VC1OUT	3'h06	●	●	●
	GPIO	3'h00	●	●	●
PA13	RXD0/SDI00/SDA00	3'h01	●	●	●
	TI05/TO05	3'h03	●	●	●
	RTC1HZ	3'h04	●	●	●
	KR4	3'h06	●	●	●
	PCLBUZ0	3'h07	●	●	●
	GPIO	3'h00	●	●	●
PA14	TXD0/SDO00	3'h01	●	●	●
	TI06/TO06	3'h03	●	●	●
	KR1	3'h06	●	●	●
	PCLBUZ1	3'h07	●	●	●
	GPIO	3'h00	●	●	●
PA15	RXD0/SDI00/SDA00	3'h01	●	●	●
	TI07/TO07	3'h03	●	●	●
	SPI0_NSS	3'h05	●	●	●
	KR0	3'h06	●	●	●
	GPIO	3'h00	●	●	●

Table 4.1.1 (4/8)

Port name	Alternate function	Digital output function setting register pxxcfg[2:0]	Function		
			64LQFP	48LQFP	40QFN
PB00	TXD1/SDO10	3'h01	●	●	●
	TI00	3'h02	●	●	●
	TO00	3'h03	●	●	●
	PCLBUZ0	3'h07	●	●	●
	GPIO	3'h00	●	●	●
PB01	SCLK20/SCL20	3'h01	●	●	●
	TI01/TO01	3'h03	●	●	●
	PCLBUZ1	3'h07	●	●	●
	GPIO	3'h00	●	●	●
PB02	TXD2/SDO20	3'h01	●	●	●
	TI02/TO02	3'h03	●	●	●
	TA_TI/TA_TO	3'h06	●	●	●
	GPIO	3'h00	●	●	●
PB03	SCLK11/SCL11	3'h01	●	●	●
	TI03/TO03	3'h03	●	●	●
	TI04_GATE	3'h04	●	●	●
	SPI0_SCK	3'h05	●	●	●
	PCLBUZ0	3'h07	●	●	●
	GPIO	3'h00	●	●	●
PB04	SDI11/SDA11	3'h01	●	●	●
	TI04/TO04	3'h03	●	●	●
	TI05_GATE	3'h04	●	●	●
	SPI0_MISO	3'h05	●	●	●
	TA_TI/TA_TO	3'h06	●	●	●
	GPIO	3'h00	●	●	●
PB05	SDO11	3'h01	●	●	●
	TI05/TO05	3'h03	●	●	●
	TI06_GATE	3'h04	●	●	●
	SPI0_MOSI	3'h05	●	●	●
	GPIO	3'h00	●	●	●
PB06	TXD0/SDO00	3'h01	●	●	●
	SCLA0	3'h02	●	●	●
	TI06/TO06	3'h03	●	●	●
	TA_TI/TA_TO	3'h06	●	●	●
	GPIO	3'h00	●	●	●

Table 4.1.1 (5/8)

Port name	Alternate function	Digital output function setting register pxxcfg[2:0]	Function		
			64LQFP	48LQFP	40QFN
PB07	RXD0/SDI00/SDA00	3'h01	●	●	●
	SDAA0	3'h02	●	●	●
	TI07/TO07	3'h03	●	●	●
	TA_TON	3'h06	●	●	●
	GPIO	3'h00	●	●	●
PB08	SCLK00/SCL00	3'h01	●	●	●
	GPIO	3'h00	●	●	●
PB09	TXD0/SDO00	3'h01	●	●	-
	SCLA0	3'h02	●	●	-
	TO00	3'h03	●	●	-
	TI07_GATE	3'h04	●	●	-
	TI00	3'h05	●	●	-
	GPIO	3'h00	●	●	-
PB10	TXD1/SDO10	3'h01	●	●	●
	SCLA0	3'h02	●	●	●
	TI02/TO02	3'h03	●	●	●
	SPI0_SCK	3'h05	●	●	●
	GPIO	3'h00	●	●	●
PB11	RXD1/SDI10/SDA10	3'h01	●	●	●
	SDAA0	3'h02	●	●	●
	TI03/TO03	3'h03	●	●	●
	TI00_GATE	3'h04	●	●	●
	GPIO	3'h00	●	●	●
PB12	TXD1/SDO10	3'h01	●	●	●
	TI04/TO04	3'h03	●	●	●
	SPI0_NSS	3'h05	●	●	●
	VC0OUT	3'h06	●	●	●
	GPIO	3'h00	●	●	●
PB13	SCLK10/SCL10	3'h01	●	●	●
	SCLA0	3'h02	●	●	●
	TI05/TO05	3'h03	●	●	●
	TI01_GATE	3'h04	●	●	●
	SPI0_SCK	3'h05	●	●	●
	GPIO	3'h00	●	●	●

Table 4.1.1 (6/8)

Port name	Alternate function	Digital output function setting register pxxcfg[2:0]	Function		
			64LQFP	48LQFP	40QFN
PB14	SS01	3'h01	●	●	●
	SDAA0	3'h02	●	●	●
	TI06/TO06	3'h03	●	●	●
	RTC1HZ	3'h04	●	●	●
	SPI0_MISO	3'h05	●	●	●
	GPIO	3'h00	●	●	●
PB15	RXD2/SDI20/SDA20	3'h01	●	●	●
	TI07/TO07	3'h03	●	●	●
	TI02_GATE	3'h04	●	●	●
	SPI0_MOSI	3'h05	●	●	●
	GPIO	3'h00	●	●	●
PC00	SS21	3'h01	●	-	-
	TI00	3'h02	●	-	-
	TO00	3'h03	●	-	-
	TI03_GATE	3'h04	●	-	-
	GPIO	3'h00	●	-	-
PC01	SCLK21/SCL21	3'h01	●	-	-
	TI01/TO01	3'h03	●	-	-
	TA_TI/TA_TO	3'h06	●	-	-
	GPIO	3'h00	●	-	-
PC02	SDI21/SDA21	3'h01	●	-	-
	TI02/TO02	3'h03	●	-	-
	SPI0_MISO	3'h05	●	-	-
	TA_TON	3'h06	●	-	-
	GPIO	3'h00	●	-	-
PC03	SDO21	3'h01	●	-	-
	TI03/TO03	3'h03	●	-	-
	SPI0_MOSI	3'h05	●	-	-
	TA_TI/TA_TO	3'h06	●	-	-
	GPIO	3'h00	●	-	-
PC04	TXD1/SDO10	3'h01	●	-	-
	TI04/TO04	3'h03	●	-	-
	PCLBUZ1	3'h07	●	-	-
	GPIO	3'h00	●	-	-

Table 4.1.1 (7/8)

Port name	Alternate function	Digital output function setting register pxxcfg[2:0]	Function		
			64LQFP	48LQFP	40QFN
PC05	RXD1/SDI10/SDA10	3'h01	●	-	-
	TI05/TO05	3'h03	●	-	-
	GPIO	3'h00	●	-	-
PC06	SCLK01/SCL01	3'h01	●	-	-
	TI06/TO06	3'h03	●	-	-
	GPIO	3'h00	●	-	-
PC07	SDI01/SDA01	3'h01	●	-	-
	TI07/TO07	3'h03	●	-	-
	KR7	3'h06	●	-	-
	GPIO	3'h00	●	-	-
PC08	SDO01	3'h01	●	-	-
	TI00	3'h02	●	-	-
	TO00	3'h03	●	-	-
	KR6	3'h06	●	-	-
	GPIO	3'h00	●	-	-
PC09	SCLK00/SCL00	3'h01	●	-	-
	TI01/TO01	3'h03	●	-	-
	KR5	3'h06	●	-	-
	GPIO	3'h00	●	-	-
PC10	TXD2/SDO20	3'h01	●	-	-
	TI02/TO02	3'h03	●	-	-
	GPIO	3'h00	●	-	-
PC11	RXD2/SDI20/SDA20	3'h01	●	-	-
	TI03/TO03	3'h03	●	-	-
	GPIO	3'h00	●	-	-
PC12	TXD2/SDO20	3'h01	●	-	-
	TI04/TO04	3'h03	●	-	-
	GPIO	3'h00	●	-	-
PC13	SCLK10/SCL10	3'h01	●	●	-
	TI05/TO05	3'h03	●	●	-
	RTC1HZ	3'h04	●	●	-
	GPIO	3'h00	●	●	-
PC14	SS10	3'h01	●	●	●
	GPIO	3'h00	●	●	●
PD00	GPIO	3'h00	●	●	●
PD01	GPIO	3'h00	●	●	-

Table 4.1.1 (8/8)

Port name	Alternate function	Digital output function setting register pxxcfg[2:0]	Function		
			64LQFP	48LQFP	40QFN
PD02	SCLK20/SCL20	3'h01	●	-	-
	TI02/TO02	3'h03	●	-	-
	GPIO	3'h00	●	-	-
PD03	RXD0/SDI00/SDA00	3'h01	●	●	●
	SDAA0	3'h02	●	●	●
	TI01/TO01	3'h03	●	●	●
	SPI0_NSS	3'h05	●	●	●
	PCLBUZ1	3'h07	●	●	●
	GPIO	3'h00	●	●	●
PD04	SCLK10/SCL10	3'h01	●	-	-
	GPIO	3'h00	●	-	-
PD05	SCLK20/SCL20	3'h01	●	-	-
	GPIO	3'h00	●	-	-
PD06	SCLA0	3'h02	●	●	-
	KR3	3'h06	●	●	-
	GPIO	3'h00	●	●	-
PD07	SCLK00/SCL00	3'h01	●	●	-
	SDAA0	3'h02	●	●	-
	KR2	3'h06	●	●	-
	GPIO	3'h00	●	●	-
PH01	TXD1/SDO10	3'h01	●	●	●
	SDAA0	3'h02	●	●	●
	GPIO	3'h00	●	●	●
PH02	RXD1/SDI10/SDA10	3'h01	●	●	●
	SCLA0	3'h02	●	●	●
	TI01/TO01	3'h03	●	●	●
	GPIO	3'h00	●	●	●
PH03	GPIO	3'h00	●	●	●
PH04	GPIO	3'h00	●	●	●
VDD	Power supply	-	●	●	●
VSS	Ground	-	●	●	●

4.2 Port alternate function

Table 4.2.1 (1/2)

Function name	I/O	Function description
ANI0 ~ ANI25	I	A/D converter analog inputs
INTP0 ~ INTP5	I	External interrupt request inputs Designation of active edges: rising edge, falling edge, double edges
VCnIN0, VCnIN1, VCnIN2	I	Comparator inputs
VCOUT0, VCOUT1	O	Comparator outputs
OPA0-DA, OPA0-FB	I/O	OPA inputs
OPA0	O	OPA outputs
KR0 ~ KR7	I	Key interrupt inputs
CLKBUZ0, CLKBUZ1	O	Clock outputs/buzzer outputs
RTC1HZ	O	Correction clock (1Hz) output for real-time clock
RESETB	I	Active-low system reset input; if the external reset is not used, it must be connected directly or through a resistor to V_{DD}.
IrRxD	I	IrDA serial data inputs
IrTxD	O	IrDA serial data outputs
RxD0 ~ RxD2	I	Serial data inputs of serial interfaces UART0, UART1, UART2
TxD0 ~ TxD2	O	Serial data outputs of serial interfaces UART0, UART1, UART2
SCL00, SCL01, SCL10, SCL11, SCL20, SCL21	O	Serial clock outputs of serial interfaces IIC00, IIC01, IIC10, IIC11, IIC20, IIC21
SDA00, SDA01, SDA10, SDA11, SDA20, SDA21	I/O	Serial data inputs/outputs of serial interfaces IIC00, IIC01, IIC10, IIC11, IIC20, IIC21
SCLK00, SCLK01, SCLK10, SCLK11, SCLK20, SCLK21	I/O	Serial clock inputs/outputs of serial interfaces SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21
SDI00, SDI01, SDI10, SDI11, SDI20, SDI21	I	Serial data inputs of serial interfaces SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21
SS00, SS01, SS10, SS11, SS20, SS21	I	Chip select inputs of serial interfaces SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21
SDO00, SDO01, SDO10, SDO11, SDO20, SDO21	O	Serial data outputs of SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21
SPINSS	I	Chip select inputs of serial interface SPI
SPISCK	I/O	Serial clock inputs/outputs of serial interface SPI
SPIMISO	I/O	Serial data inputs/outputs of serial interface SPI
SPIMOSI	I/O	Serial data inputs/outputs of serial interface SPI

Table 4.2.1 (2/2)

Function name	I/O	Function description
SCLA0	I/O	Serial clock inputs/outputs of serial interface IICA0
SDAA0	I/O	Serial data inputs/outputs of serial interface IICA0
TI00 ~ TI07	I	16-bit Timer8 external counting clock/capture trigger inputs
TO00 ~ TO07	O	16-bit Timer8 outputs
TI00_GATE~TI07_GATE	I	16-bit Timer8 gate inputs
TA_TO	O	Timer A outputs
TA_TI	I	Timer A inputs
TA_TON	O	Timer A reverse outputs
X1, X2	—	Resonators for main system clock connection
EXCLK	I	External clock inputs for main system clock
XT1, XT2	—	Resonators for slave system clock connection
EXCLKS	I	External clock inputs for subsystem clock
VDD	—	Power supply
AVREFP	I	Positive (+) reference voltage inputs for A/D converter
AVREFM	I	Negative (-) reference voltage inputs for A/D converter
VSS	—	Ground
SWDIO	I/O	SWD data interface
SWCLK	I	SWD clock interface

Remark: As a measure against noise and lock-up, a bypass capacitor (approximately 0.1μF) must be connected between V_{DD} and V_{SS} with the shortest possible distance and using thicker wiring. (n=0, 1)

5 Function Summary

5.1 ARM® Cortex®-M0+ core

The ARM Cortex-M0+ processor is the latest generation of ARM processors designed for embedded systems. It offers a low-cost platform aimed at meeting the needs of microcontrollers with few pins and low power consumption while delivering excellent computing performance and advanced system interrupt response.

The Cortex-M0+ is a 32-bit RISC processor that provides superior code efficiency and high-performance expectations compared to 8-bit and 16-bit devices of similar memory size. It features 32 address lines, allowing for up to 4GB of memory space.

The BAT32G127 incorporates the embedded ARM core, making it compatible with all ARM tools and software.

5.2 Memory

5.2.1 Flash memory

The BAT32G127 has a built-in flash memory that can be programmed, erased and rewritten. It has the following features:

- Programs and data share 128K storage.
- 2.5KB dedicated data Flash memory.
- Support page erasure, the size of each page is 512byte, and erase time is 4ms.
- Support byte/half-word/word (32bit) programming, and the programming time is 24us.

5.2.2 SRAM

The BAT32G127 contains 8KB of embedded SRAM.

5.3 Enhanced DMA controller

It has a built-in enhanced DMA (Direct Memory Access) controller that enables data transfer between memories without using the CPU.

- Support DMA boot by peripheral function interrupts, enabling real-time control by communication, timer and A/D.
- The transfer source/target field is optional for the full address space range (when the flash field is used as the target address, the flash needs to be preset to the programming mode).
- Support 4 modes (normal transfer mode, repeat transfer mode, block transfer mode and chain transfer mode).

5.4 Linkage controller

The linkage controller links the output events by each peripheral function with the peripheral function trigger sources. This enables collaborative operation between peripheral functions without using the CPU.

The linkage controller has the following functions:

- It can link event signals together to realize the linkage of peripheral functions.
- There are 16 types of event input and 6 types of event triggering.

5.5 LCD controller/driver

The LCD supports 4COM*42SEG/6COM*40SEG/8COM*38SEG

Functions are as follows:

- Waveform A or waveform B can be selected.
- LCD driver voltage generation circuit can switch between internal boost, capacitor split and external resistance division.
- Automatically output segment signals and common signals by automatically reading the display data register.
- Can select from 16 reference voltages (contrast adjustment) generated when the boost circuit is running.
- Enable LCD blinking display.

5.6 Clock generation and startup

A clock generation circuit is a circuit that generates a clock to the CPU and peripheral hardware. There are three types of system clocks and clock oscillation circuits.

5.6.1 Main system clock

- X1 oscillation circuit: The resonator can be connected to pins (X1 and X2) to generate a clock oscillation of 1~20MHz, and the oscillation can be stopped by executing a deep sleep command or setting MSTOP.
- High-speed on-chip oscillator (high-speed OCO): Oscillation can be performed by selecting the frequency by the option byte. After released, the CPU starts running at this high-speed on-chip oscillator clock by default. Oscillation can be stopped by executing a deep sleep command or setting the HIOSTOP bit. The frequency set by the option byte can be changed through the frequency selection register of the high-speed on-chip oscillator. The maximum frequency is 32MHz with an accuracy ±1.0%.
- Input external clock from pin (X2): (1~20MHz), and the input of the external main system clock can be invalidated by executing a deep sleep command or setting the MSTOP bit.

5.6.2 Subsystem clock

- XT1 oscillator circuit: A 32.768kHz clock oscillation can be generated by connecting a 32.768kHz resonator to the pins (XT1 and XT2), and the oscillation can be stopped by setting the XTSTOP bit.
- An external clock input by the pin (XT2): 32.768kHz, and the external clock input can be disabled by setting the XTSTOP bit.

5.6.3 Low-speed on-chip oscillator clock

- Low-speed on-chip oscillator (low-speed OCO): generate a 32kHz (TYP.) clock oscillation. The low-speed on-chip oscillator clock cannot be used as the CPU clock. Only the following peripheral hardware can run off the low-speed on-chip oscillator clock:
- Watchdog timer (WWDT)
- Real time clock (RTC)
- 15-bit interval timer

5.7 Power management

5.7.1 Power supply mode

V_{DD}: External power supply, voltage range: 1.8 to 5.5V.

5.7.2 Power-on reset

The power-on reset circuit (POR) has the following functions.

- An internal reset signal is generated when power is applied. If the supply voltage (V_{DD}) is greater than the detection voltage (V_{POR}), the reset is released. However, the reset state must be maintained by a voltage detection circuit or an external reset until the operating voltage range is reached.
- Compare the supply voltage (V_{DD}) and the detection voltage (V_{POR}), when $V_{DD} < V_{POR}$, an internal reset signal is generated. However, when the power supply drops, it must be shifted to the deep sleep mode or set to the reset state by the voltage detection circuit or external reset before falling below the operating voltage range. If operation is to be restarted, it must be verified that the power supply voltage has returned to within the operating voltage range.

5.7.3 Voltage detection

The voltage detection circuit sets the operating mode and detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) via option bytes. The voltage detection (LVD) circuit has the following functions:

- Compare the supply voltage (V_{DD}) and the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) and generate an internal reset or interrupt request signal.
- The sense voltage of the supply voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can be selected by option bytes.
- Can run in deep sleep mode.
- When the power supply rises, it must be maintained in the reset state by voltage detection circuitry or an external reset before reaching the operating voltage range. When the power supply drops, it must be switched to deep sleep mode before it is less than the operating voltage range, or set to reset by voltage detection circuit or external reset.
- The operating voltage range varies depending on the setting of user option bytes.

5.8 Low-power mode

The BAT32G127 supports two low-power modes to achieve the best compromise between low power consumption, short start-up time, and available wake-up sources:

- Sleep mode: Sleep mode is entered by executing the sleep instruction. Sleep mode is a mode to stop the CPU running clock. If the high-speed system clock oscillator circuit or the high-speed on-chip oscillator is oscillating before the sleep mode is set, each clock continues to oscillate. Although this mode does not allow the operating current to be reduced to the level of deep sleep mode, it is an effective mode when processing is to be restarted immediately by an interrupt request or when frequent intermittent operation is to be performed.
- Deep sleep mode: Deep sleep mode is entered by executing the deep sleep instruction. Deep sleep mode is a mode that stops the oscillation of the high-speed system clock oscillator and high-speed on-chip oscillator and stops the whole system. The operating current of the chip can be greatly reduced. Since the deep sleep mode can be canceled by an interrupt request, intermittent operation is also possible. However, in the case of the X1 clock, since it is necessary to wait for the oscillation to stabilize when releasing the deep sleep mode, it is necessary to select the sleep mode if it is necessary to start processing immediately by an interrupt request.

In any of these modes, the registers, flags, and data memories remain as they were before being set to standby mode, and the status of the output latches and output buffers of the input/output ports is also maintained.

5.9 Reset function

A reset signal can be generated by the following seven methods:

(1) An external reset is input via the RESETB pin.
(2) An internal reset is generated by programmed runaway detection of the watchdog timer.
(3) An internal reset is generated by comparing the supply voltage and the detection voltage of POR.
(4) An internal reset is generated by comparing the supply voltage and the detection voltage of LVD.
(5) An internal reset is generated by a RAM parity error.
(6) An internal reset is generated by accessing to the illegal memory.
(7) Software reset

The internal reset is the same as the external reset, and after the reset signal is generated, the procedure is executed from the addresses written in 0000H and 0001H.

5.10 Interrupt function

The Cortex-M0+ processor has a built-in Nested Vector Interrupt Controller (NVIC) that supports up to 32 interrupt request (IRQ) inputs, a non-maskable interrupt (NMI) input, and multiple internal exceptions.

The product handles 32 maskable interrupt requests (IRQs) and 1 non-maskable interrupt (NMI), as described in the corresponding section of the User's Manual. The actual number of interrupt sources varies by product.

5.11 Real-time clock (RTC)

Functions of real-time clock (RTC) are show as below.

- Holds counters for years, months, weeks, days, hours, minutes, and seconds
- Fixed cycle break (cycles: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm clock interrupt (alarm clock: week, hour, minute)
- 1Hz pin out capability
- Support prescalers of subsystem clock or main system clock as RTC operation clocks.
- Real-time clock interrupt signals (INTRTC) can be used to wake up in deep sleep mode.
- Watch error correction with high accuracy

Year, month, week, day, hour, minute and second counters are only available if the subsystem clock (32.768kHz) or main system clock prescaler is selected as the RTC operation clock. When the low-speed on-chip oscillator clock (32kHz) is selected, only the fixed-cycle interrupt function can be used.

5.12 Watchdog timer

The 1- channel WWDT and 17-bit watchdog timer operation are set by option byte count. The watchdog timer operates on a low-speed on-chip oscillator clock (32KHz). The watchdog timer is used to detect program instability. When program instability is detected, an internal reset signal is generated.

The following are judged to be program instability:

- When the watchdog timer counter overflows
- When a bit operation instruction is executed on the watchdog timer enable register (WDTE)
- When writing data other than "ACH" to the WDTE register
- When writing data to the WDTE register during window closure

5.13 SysTick timer

This timer is exclusive to real-time operating systems, but can also be used as a standard decrement counter.

It is characterized by the generation of a maskable system interrupt when the 24-bit decrementing counter self-loading capacity counter reaches zero.

5.14 Timer8

This product has a built-in Timer8, a timer unit containing an 8-channel 16-bit timer. Each 16-bit timer is called a “channel” and can be used as an independent timer or in combination with multiple channels for advanced timer functions.

For details of each function, refer to the table below.

Independent channel operation function	Multi-channel linkage operation function
● Interval timer ● Square wave output ● External event counter ● Frequency divider ● Input pulse interval measurement ● Input signal high/low width measurement ● Delay counter	● Single trigger pulse output ● PWM output ● Multiple PWM output

5.14.1 Independent channel operation function

The independent channel operation function is a function that allows you to use any channel independently of other channel operation modes. The independent channel operation function is used in the following modes:

(1) Interval timer: It can be used as a reference timer for generating interrupts at fixed intervals (INTTM).

(2) Square wave output: Whenever an INTTM interrupt is generated, a flip is triggered to output a 50% duty cycle square wave from the timer output pin (TO).

(3) External event counter: Count the effective edge of the input signal of the timer input pin (TI) and can be used as an event counter to generate an interrupt if the specified number of times is reached.

(4) Divider function (limited to channel 0 of unit 0): divide the input clock of the timer input pin (TI00) and output it from the output pin (TO00).

(5) Measurement of input pulse interval: The interval between input pulses is measured by starting counting at the effective edge of the input pulse signal at the timer input pin (TI) and capturing the count value at the effective edge of the next pulse.

(6) High/low width measurement of input signal: Measure the high or low width of the input signal by starting counting on one edge of the input signal of the timer input pin (TI) and capturing the count value on the other edge.

(7) Delay counter: Starts counting at the effective edge of the input signal at the timer input pin (TI) and generates an interrupt after an arbitrary delay period has elapsed.

5.14.2 Multi-channel linkage operation function

The multi-channel linkage operation function is a function that combines the master channel (the reference timer for the main control period) and the slave channel (the timer that follows the operation of the master channel). The multi-channel linkage function can be used in the following modes:

(1) Single trigger pulse output: Two channels are used in pairs to generate a single trigger pulse that can arbitrarily set the output timing and pulse width.

(2) PWM (Pulse Width Modulation) output: Two channels are used in pairs to generate pulses that can set the period and duty cycle arbitrarily.

(3) Multiple PWM (Pulse Width Modulation) output: Up to 7 PWM signals of any duty cycle can be generated at a fixed period by expanding the PWM function and using one master channel and multiple slave channels.

5.14.3 8-bit timer operation function

The 8-bit timer operation function uses the 16-bit timer channel as the function of two 8-bit timer channels. (Only Channel 1 and Channel 3 can be used).

5.14.4 LIN-bus support function

The Timer8 (channel 3 only) unit can be used to check whether the received signal in the LIN-bus communication is suitable for the LIN-bus communication format.

1) Wake-up signal detection: The low-level width is measured by starting counting on the falling edge of the input signal on the UART serial data input pin (RxD) and capturing the count value on the rising edge. If the low width is greater than or equal to a fixed value, it is considered a wake-up signal.

2) Detection of the break field: After a wake-up signal is detected, the low-level width is measured by starting counting from the falling edge of the input signal of the UART serial data input pin (RxD) and capturing the count value on the rising edge. If the width of the low level is greater than or equal to a fixed value, it is considered to be a break field.

3) Measurement of sync field pulse width: After detecting the break field, measure the low- and high-level widths of the input signal of the UART serial data input pin (RxD). The baud rate is calculated from the bit interval of the synchronization field measured in this way.

5.15 TimerA

Timer A is a 16-bit timer capable of pulse output, measuring the width and period of external input pulses, and counting external events.

The 16-bit timer consists of a reload register and a down-counting counter. The reload register and the down-counting counter share the same address. Accessing the TA0 register allows access to both the reload register and the counter.

5.16 15-bit interval timer

This product has a built-in 15-bit interval timer that generates interrupts (INTIT) at any pre-set time interval, which can be used to wake up from deep sleep mode.

5.17 Clock output/buzzer output controller

The clock output controller is used to provide a clock to the peripheral ICs, and the buzzer output controller is used to output a square wave at the buzzer frequency. The clock output or buzzer output is realized by dedicated pins.

5.18 Universal serial communication unit

This product has a built-in general-purpose serial communication unit, and each unit has up to 8 serial communication channels. It can realize standard SPI, simplified SPI, UART and simple I^2C communication functions. Taking the 64-pin product as an example, the functions of each channel are assigned as follows.

5.18.1 3-wire serial interface (SSPI)

Data is transmitted and received synchronously with the serial clock (SCK) output of the master device.

This is a clock-synchronous communication interface that communicates using a total of three communication lines: one serial clock (SCK), one transmit serial data (SO), and one receive serial data (SI).

[Data transmission and reception]

- Data length of 7 to 16 bits
- Phase control of data transmission and reception
- MSB/LSB first
- Level setting for transmitting and receiving data

[Clock control]

- Master or slave selection
- Phase control of input/output clock

- Transfer cycles generated by prescalers and channel internal counters
- Maximum transfer rate

  Master communication: Max. $F_{CLK}/2$

  Slave communication: Max. $F_{MCK}/6$

[Interrupt function]

- Transfer end interrupt, buffer null interrupt

[Error detection flag]

- Overflow error

5.18.2 UART

This function enables asynchronous communication over two lines, serial data transmission (TxD) and serial data reception (RxD). Using these two communication lines, data is transmitted and received asynchronously (using the internal baud rate) with other communicating parties in the data frame (consisting of start bits, data, parity bits, and stop bits). Full-duplex UART communication can be implemented by using two channels, dedicated transmitting (even channels) and dedicated receiving (odd channels), and LIN-bus can also be supported by combining a Timer8 unit and an external interrupt (INTP0).

[Data transmission and reception]

- Data length of 7, 8, 9 or 16 bits
- MSB/LSB first
- Level setting for transmitting and receiving data, selection of reverse phase
- Parity bit appending, parity check function
- Stop bit appending

[Interrupt function]

- Transfer end interrupt and buffer null interrupt
- Frame error and parity check error

[Error detection flag]

- Frame error, parity error, overflow error

[LIN-bus function]

- Detection of wake-up signal
- Detection of break field (BF)
- Measurement of synchronous field, calculation of baud rate

5.18.3 Simplified I²C

It is a function to synchronize clock communication with multiple devices through two lines of serial clock (SCL) and serial data (SDA). Since this simplified I²C is designed for single communication with devices such as Flash memory, and A/D converters, it is used only as a master device. The start and stop conditions, like the operation control registers, must comply with the AC characteristics and are handled by the software.

[Data transmission and reception]

- Master transmission, master reception (limited to the master function of single master)
- ACK output function, ACK detection function
- 8-bit data length (when transmitting the addresses, specify the addresses with the highest 7 bits, and use the lowest bit for R/W control)
- Start and stop conditions are generated by software

[[Interrupt function]

- Transfer end interruption

[Error detection flag]

- ACK error, overflow error

[Simplified I²C unsupported features]

- Slave transmission, slave reception
- Multi-master function (arbitration failure detection function)
- Wait detection function

5.19 Standard serial interface SPI

The standard serial interface SPI has the following two modes:

1) Run-stop mode: This is the mode used when serial transfer is not performed, which reduces power consumption.
2) 3-wire serial I/O mode: This mode transmits 8-bit or 16-bit data to multiple devices over 3 wires of a serial clock (SCK) and 2 serial data buses (MISO and MOSI).

5.20 Standard serial interface IICA

The serial interface IICA has the following three modes:

1) Run-stop mode: This is the mode used when serial transfer is not performed, which reduces power consumption.
2) I^2C bus mode (support multi-master): This mode transmits 8-bit data to multiple devices over 2 wires of a serial clock (SCLA) and a serial data bus (SDAA). In accordance with the I2C bus format, the master device can generate “start conditions”, “address”, “indication of transmission direction”, “data” and “stop conditions” on the serial data bus for the slave devices. The slave device automatically detects the received status and data by hardware. This feature simplifies the I^2C bus control part of the application program. Since the SCLA and SDAA pins of the serial interface IICA are used as open drain outputs, pull-up resistors are required for the serial clock line and the serial data bus.
3) Wake-up mode: In deep sleep mode, when an extension code or a local station address is received from the master device, the deep sleep mode can be released by generating an interrupt request signal (INTIICA). This is set via the IICA control register.

5.21 Analog-to-digital converter (ADC)

This product has a built-in 12-bit resolution analog-to-digital converter, SARADC, which converts analog inputs to digital values and controls the A/D conversion of up to 26 analog channels (ANI0~ANI25).

The ADC contains the following functions:

- 12-bit resolution, slew rate: 0.71Msps.
- Triggering mode: support software triggering, hardware triggering and hardware triggering in standby state.
- Channel selection: support single-channel select mode and multi-channel scan mode.
- Conversion mode: support single conversion and continuous conversion.
- Operating voltage: support $1.8V \leqslant V_{DD} \leqslant 5.5V$ operating voltage range.
- It can detect the built-in reference voltage (1.45V) and temperature sensors.

The ADC can set various A/D conversion modes by combining the modes described below.

Trigger mode	Software trigger	Start the conversion by operating the software.
	Hardware-trigger no-wait mode	The conversion is started by detecting a hardware trigger.
	Hardware trigger wait mode	In the conversion standby state when the power is cut off, the power is turned on by detecting the hardware trigger, and the conversion starts automatically after the A/D power stabilization waiting time.
Channel select mode	Select mode	Select 1 channel of analog input for A/D conversion.
	Scan mode	Four consecutive channels can be selected as analog inputs for sequential A/D conversion. Four consecutive channels from ANI0 to

		ANI25 can be selected as analog inputs.
Conversion mode	Single conversion mode	Perform an A/D conversion for the selected channel.
	Continuous conversion mode	Perform continuous A/D conversions for the selected channel until stopped by the software.
Sample time/ conversion time	Number of sample clocks/ conversion clocks	The sampling time can be set by register, the default value of sampling clock number is 13.5 clk, and the minimum value of conversion clock number is 31.5 clk.

5.22 Digital-to-analog converter (D/A)

The D/A converter is an 8-bit resolution converter that converts digital inputs to analog signals and controls the analog outputs. It has the following functions.

- 8-bit resolution
- R-2R ladder network
- Analog output voltage
  8-bit resolution: V_{DD}*m8/256 (m8: DACSi register set value)
- Operation modes
  Normal mode, real-time output mode

Remark: i=0

5.23 Operational amplifier (OPA)

This product includes an operational amplifier (OPA) with the following features:

- Supports rail-to-rail operation
- The OPA can operate in constant current mode or buffer mode; the buffer mode can be used to test OPA offset
- The negative feedback terminal of the OPA supports either an internal constant current resistor or an external pin OPA_FB
- The analog input at the positive terminal of the OPA can be selected from either the built-in 5-bit DAC of the op-amp module or the 8-bit DAC provided with this product
- The output of the OPA can be used as an analog input for the A/D converter or as a positive terminal analog input for the comparator 0 (CMP0)

5.24 Comparator (CMP)

This product has built-in two-channel comparators CMP0 and CMP1 with the following features:

- Can select comparator high speed mode, comparator low speed mode, or comparator window mode.
- The external reference input and internal reference voltage can be selected for the reference voltage.
- The cancellation width of the noise cancellation digital filter can be selected.
- Can detect the active edge of the comparator output and generate an interrupt signal.
- Can detect the active edge of the comparator output and output the event signal to the linkage controller.

5.25 Two-wire serial debug port (SW-DP)

The ARM's SW-DP interface allows connection to the microcontroller via a serial line debugging tool.

5.26 Safety functions

5.26.1 Flash CRC function (high-speed CRC, universal CRC)

This detects data errors in the flash memory by performing CRC operations.

The following two CRCs can be used according to the application or purpose of use.

- High-speed CRC: During the initialization routine, it can stop the CPU and check the entire code flash area at high speed.
- Universal CRC: This can be used for multi-purpose checking during CPU operation, not limited to the code flash area.

5.26.2 RAM parity error detection function

This detects parity errors when reading RAM data.

5.26.3 SFR guard function

This prevents SFRs from being rewritten when the CPU freezes.

5.26.4 Illegal memory access detection function

This detects illegal access to a invalid memory areas (asuch as areas where no memory is allocated and areas to which access is restricted).

5.26.5 Frequency detection function

Able to use the Timer8 unit to self-test the CPU or peripheral hardware clock frequencies.

5.26.6 A/D test function

The A/D converter is self-tested by A/D converting the positive (+) reference voltage, the negative (-) reference voltage, the analog input channel (ANI), the temperature sensor output voltage, and the internal reference voltage.

5.26.7 Digital output signal level detection function for input/output ports

When the input/output port is in output mode, the output level of the pin can be read.

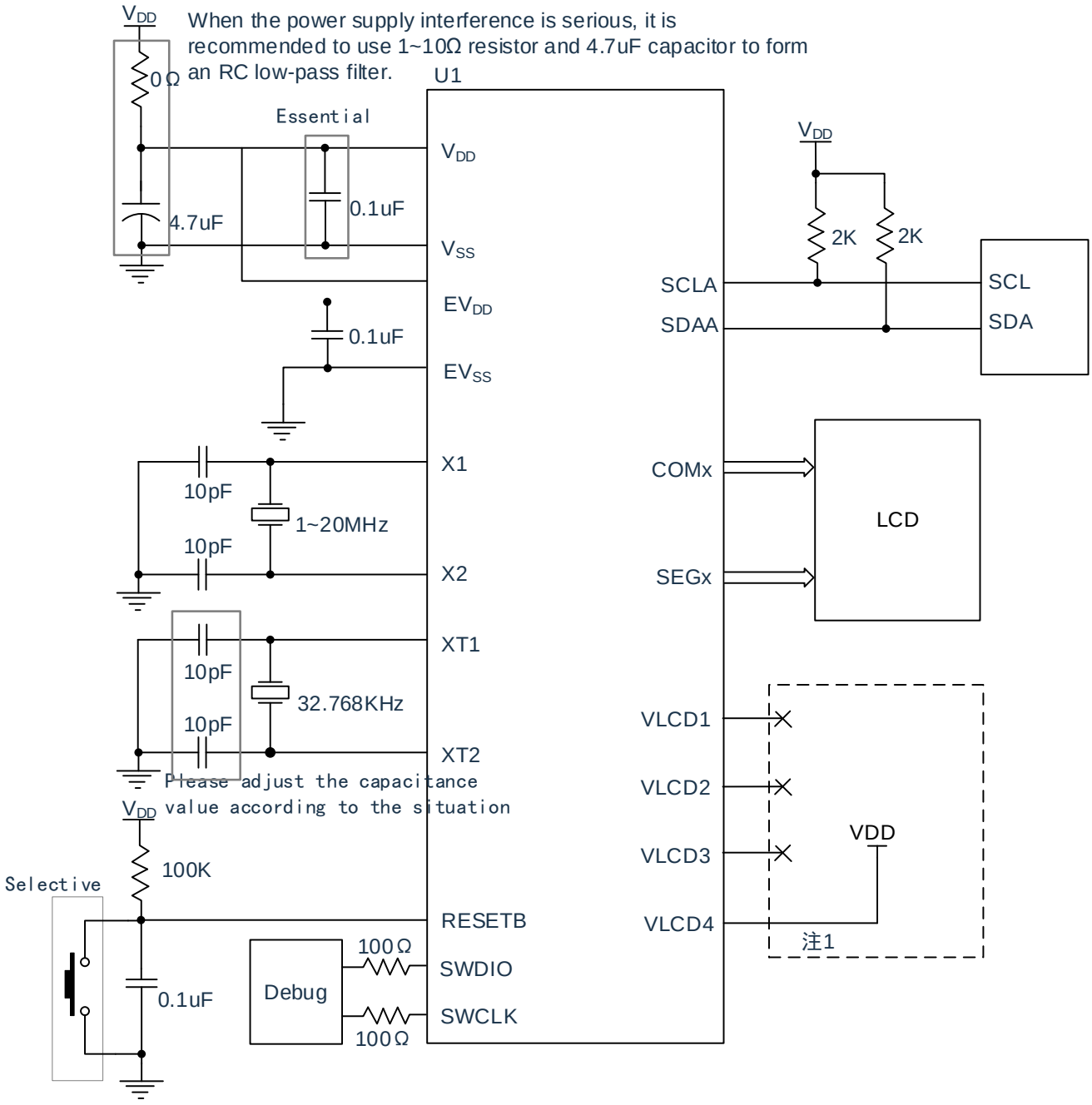
5.27 Key function

A key interrupt (INTKR) can be generated by inputting the falling edge of the key interrupt input pins (KR0~KR7).

6 Electrical Characteristics

6.1 Typical application peripheral circuit

The reference diagram for the connection of peripheral circuits for typical MCU applications is as follows:



Note 1: This connection is for internal resistor voltage divider. For more information about LCD driver power generation, please refer to section 19.6 in User Manual.

6.2 Absolute maximum voltage ratings

Absolute maximum voltage ratings (1/2) (T_A= -40~105℃)

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	-	-0.5~+6.5	V
Input voltage	V_I	PA00~PA15, PB00~PB15, PC00~PC14 PD00~PD07, PH01~PH04, RESETB/PH00	-0.3~V_{DD}+0.3 Note 1	V
Output voltage	V_O	PA00~PA15, PB00~PB15, PC00~PC14 PD00~PD07, PH00-PH04	-0.3~V_{DD}+0.3 Note 1	V
Analog input voltage	V_{AI}	ANI0~ANI25	-0.3~V_{DD}+0.3 and -0.3~AV_{REF}(+)+0.3 Note 1,2	V

Note 1: No more than 6.5V.

Note 2: The pin of the A/D conversion target cannot exceed AV_{REF} (+)+0.3.

Caution: Even if one item in each item instantly exceeds the absolute maximum rating, it may reduce the quality of the product. The absolute maximum ratings are the ratings that may cause physical damage to the product, and the product must be used in a state that do not exceed the ratings.

Remark:

1. Unless otherwise specified, the characteristics of alternate-function pins are the same as the characteristics of the port pins.
2. AV_{REF}(+): A/D converter positive (+) reference voltage
3. V_{SS}: Reference voltage.
4. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

Absolute maximum voltage ratings (2/2) (T_A= -40~105°C)

Item	Symbol	Condition		Rating	Unit
LCD voltage	V_{LI1}	V_{L1} input voltage Note 1		-0.3~+2.8	V
	V_{LI2}	V_{L2} input voltage Note 1		-0.3~+6.5	V
	V_{LI3}	V_{L3} input voltage Note 1		-0.3~+6.5	V
	V_{LI4}	V_{L4} input voltage Note 1		-0.3~+6.5	V
	V_{LI5}	CAPL, CAPH input voltage Note 1		-0.3~+6.5	V
	V_{LO1}	V_{L1} output voltage		-0.3~+6.5	V
	V_{LO2}	V_{L2} output voltage		-0.3~+6.5	V
	V_{LO3}	V_{L3} output voltage		-0.3~+6.5	V
	V_{LO4}	V_{L4} output voltage		-0.3~+6.5	V
	V_{LO5}	CAPL, CAPH output voltage Note 1		-0.3~+6.5	V
	V_{LO6}	COM0~COM7, SEG0~SEG41 output voltage	External resistance division method	-0.3~V_{DD}+0.3 Note 2	V
			Capacitor split method	-0.3~V_{DD}+0.3 Note 2	V
			Internal voltage boosting method	-0.3~V_{LI4}+0.3 Note 2	V

Note 1: These values are the absolute maximum ratings specified when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins, and are not the recommended applied voltage values. In the case of the internal voltage boosting method and the capacitor split method, the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins must be connected to V_{SS} by a capacitor (0.47uF±30%), and a capacitor (0.47uF±30%) must also be connected between the CAPL pin and the CAPH pin.

Note 2: No more than 6.5V.

Remark: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.3 Absolute maximum current ratings

(T_A= -40~105℃)

Item	Symbol	Condition		Rating	Unit
Output current, high	I_{OH1}	Per pin	PA00~PA15, PB00~PB15, PC00~PC14 PD00~PD07, PH00~PH02	-40	mA
		Total of all pins -170mA	PA00~PA01, PB00~PB07	-70	mA
			PB00~PB07, PC00~PC01	-100	mA
	I_{OH2}	Per pin	PH03~PH04	-3	mA
		Pin total		-15	mA
Output current, low	I_{OL1}	Per pin	PA00~PA14, PB00~PB14, PC00~PC14 PD00~PD07, PH00~PH02	40	mA
		Total of all pins 170mA	PA00~PB01, PA00~PB07	100	mA
			PB00~PB07, PD00~PD01	120	mA
	I_{OL2}	Per pin	PH03~PH04	15	mA
		Total of all pins		45	mA
Operating ambient temperature	T_A	In normal operation mode		-40~105	℃
		In flash memory programming mode			
Storage temperature	T_{stg}	-		-65~150	℃

Caution: Even if one item in each item instantly exceeds the absolute maximum rating, it may reduce the quality of the product. The absolute maximum rating is the rating that may cause physical damage to the product, and the product must be used in a state that do not exceed the ratings.

Remark:

1. Unless otherwise specified, the characteristics of alternate-function pins are the same as the characteristics of the port pins.
2. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.4 Oscillation circuit characteristics

6.4.1 X1, XT1 characteristics

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Resonator	Condition	Min.	Typ.	Max.	Unit
X1 clock oscillation frequency (F_X)	Ceramic/crystal resonator	-	1.0	-	20.0	MHz
X1 clock oscillation stabilization time	Ceramic/crystal resonator	20MHz, C=10pF	-	15	-	ms
X1 clock oscillation feedback resistor	Ceramic/crystal resonator	-	0.6	-	1.8	MΩ
XT1 clock oscillation frequency (F_{XT})	Crystal resonator	-	32	32.768	35	KHz
XT1 clock oscillation stabilization time	Crystal resonator	32.768KHz, C=10pF	-	2	-	s

Remark:

1. It only indicates the frequency tolerance range of the oscillation circuit, and the instruction execution time should be referred to the AC characteristics.
2. Please ask the resonator manufacturer to evaluate the circuit after installation, and use it after confirming the oscillation characteristics.
3. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.4.2 On-chip oscillator characteristics

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Resonator	Condition	Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency (F_{IH})Note 1,2	-	1.0	-	32.0	MHz
High-speed on-chip oscillator stabilization time (T_{SU})	-	-	12	-	us
High-speed on-chip oscillator clock frequency accuracy	T_A= 0~70℃	-2.5	-	+2.5	%
	T_A= -10~105℃	-4.5	-	+4.5	%
	T_A= -40~105℃	-7.0	-	+7.0	%
Low-speed on-chip oscillator clock frequency (F_{IL})	-	26.214	32.0	39.322	KHz

Note 1: Select the frequency of the high-speed on-chip oscillator via option bytes.

Note 2: It only indicates the characteristics of the oscillation circuit, so please refer to the AC characteristics for the instruction execution time.

Remark: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.5 DC characteristics

6.5.1 Pin characteristics

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS} =0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output current, high[Note 1]	I_{OH1}	PA00~PA15, PB00~PB15 PC00~PC14, PD00~PD07 PH00~PH02 Per pin	1.8V≤EV_{DD}≤5.5V -40~85℃	-	-	-12.0[Note 2]	mA
			1.8V≤EV_{DD}≤5.5V 85~105℃	-	-	-6.0[Note 2]	
		PA14~PA15, PB03~PB09, PC00~PC03, PC10~PC14, PD00~PD03, PH00~PH02 Total (when duty cycle≤ 70%[Note3])	4.0V≤V_{DD}≤5.5V 40~85℃	-	-	-50.0	mA
			4.0V≤EV_{DD}≤5.5V 85~105℃	-	-	-30.0	
			2.4V≤V_{DD}<4.0V	-	-	-15mA	mA
			1.8V≤V_{DD}<2.4V	-	-	-10mA	mA
		PA00~PA13, PB00~PB02, PB10~PB15, PC04~PC09, PD04~PD07 Total (when duty cycle≤ 70%[Note3])	4.0V≤V_{DD}≤5.5V 40~85℃	-	-	-50.0	mA
			4.0V≤EV_{DD}≤5.5V 85~105℃	-	-	-30.0	
			2.4V≤V_{DD}<4.0V	-	-	-15mA	mA
			1.8V≤V_{DD}<2.4V	-	-	-10mA	mA
		Total (when duty cycle≤ 70%[Note3])	4.0V≤V_{DD}≤5.5V 40~85℃	-	-	-100.0	mA
			4.0V≤EV_{DD}≤5.5V 85~105℃	-	-	-60.0	
			2.4V≤V_{DD}<4. 0V	-	-	-30mA	
			1.8V≤V_{DD}<2. 4V	-	-	-20mA	
	I_{OH2}	PH03 ~ PH04 Per pin	1.8V≤EV_{DD}≤5.5V	-	-	-2.5[Note 2]	mA
		Total (when duty cycle≤ 70%[Note3])	1.8V≤EV_{DD}≤5.5V	-	-	-5	mA

Note 1: This is the value of current that guarantees the operation of the device even if current flows from the V_{DD} pin to the output pins.

Note 2: The total current value cannot be exceeded.

Note 3: This is the output current value for the “Duty cycle ≤ 70% condition”.

The following formula can be used to calculate the output current value when the duty cycle is changed to >70% (when the duty cycle is changed to n%).

• Total pin output current=(I_{OH}×0.7)/(n×0.01)

<Calculation example> I_{OH} =-10.0mA, n =80%

Total pin output current = (-10.0×0.7)/(80×0.01)≈-8.7mA

The current at each pin does not vary by duty cycle and will not flow above the absolute maximum rating.

Caution: Setting to N-channel open drain mode will not output a high level.

Remark:

1. Unless otherwise specified, the characteristics of alternate-function pins are the same as the characteristics of the port pins.
2. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

(T_A= -40~105℃, 1.8V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS} =0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output current, low[Note 1]	I_{OL1}	PA00~PA15, PB00~PB15 PC00~PC14, PD00~PD07 PH00~PH02 Per pin	1.8V≤EV_{DD}≤5.5V -40~85℃	-	-	30[Note 2]	mA
			1.8V≤EV_{DD}≤5.5V 85~105℃	-	-	15[Note 2]	
		PA14~PA15, PB03~PB09, PC00~PC03, PC10~PC14, PD00~PD03, PH00~PH02 Total (when duty cycle≤ 70%[Note3])	4.0V≤V_{DD}≤5.5V 40~85℃	-	-	60	mA
			4.0V≤EV_{DD}≤5.5V 85~105℃	-	-	45	
			2.4V≤V_{DD}<4. 0V	-	-	25	mA
			1.8V≤V_{DD}<2. 4V	-	-	15	mA
		PA00~PA13, PB00~PB02, PB10~PB15, PC04~PC09, PD04~PD07 Total (when duty cycle≤ 70%[Note3])	4.0V≤V_{DD}≤5.5V 40~85℃	-	-	60	mA
			4.0V≤EV_{DD}≤5.5V 85~105℃	-	-	45	
			2.4V≤V_{DD}<4. 0V	-	-	25	mA
			1.8V≤V_{DD}<2. 4V	-	-	15	mA
		Total (when duty cycle≤ 70%[Note3])	4.0V≤V_{DD}≤5.5V 40~85℃	-	-	120	mA
			4.0V≤EV_{DD}≤5.5V 85~105℃	-	-	90	
			2.4V≤V_{DD}<4. 0V	-	-	50	
			1.8V≤V_{DD}<2. 4V	-	-	30	
	I_{OL2}	PH03 ~ PH04 Per pin	1.8V≤EV_{DD}≤5.5V	-	-	8[Note 2]	mA
		Total (when duty cycle≤ 70%[Note3])	1.8V≤EV_{DD}≤5.5V	-	-	15	mA

Note 1: This is the value of current that guarantees the operation of the device even if current flows from the output pins to the V_{SS} pin.

Note 2: The total current value cannot be exceeded.

Note 3: This is the output current value for the “Duty cycle ≤ 70% condition”.

The following formula can be used to calculate the output current value when the duty cycle is changed to >70% (n% duty cycle).

• Total output current = (I_{OL}×0.7)/(n×0.01)

<Calculation example> I_{OL}= 10.0mA, n = 80%

Total output current = (10.0×0.7)/(80×0.01)≈8.7mA

The current at each pin does not vary by duty cycle and will not flow above the absolute maximum

rating.

Remark:

1. Unless otherwise specified, the characteristics of alternate-function pins are the same as the characteristics of the port pins.
2. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power supply input voltage	V_{DD} EV_{DD}	-		1.8	-	5.5	V
Power ground input voltage	V_{SS} EV_{SS}	-		-0.3	-	-	V
Input voltage, high	V_{IH1}	PA00~PA15, PB00~PB15 PC00~PC14, PD00~PD07 PH00~PH04	Schmitt input	0.8V_{DD}	-	V_{DD}	V
Input voltage, low	V_{IL1}	PA00~PA15, PB00~PB15 PC00~PC14, PD00~PD07 PH00~PH04	Schmitt input	0	-	0.2V_{DD}	V

Caution: Setting to N-channel open drain mode will not output a high level.

Remark:

1. Unless otherwise specified, the characteristics of alternate-function pins are the same as the characteristics of the port pins.
2. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output voltage, high	V_{OH1}	PA00~PA15, PB00~PB15 PC00~PC14, PD00~PD07 PH00~PH02	4.0V≤V_{DD}≤5.5V I_{OH1}= -12.0mA	V_{DD}-1.5	-	-	V
			4.0V≤V_{DD}≤5.5V I_{OH1}= -6.0mA	V_{DD}-0.7	-	-	V
			2.4V≤V_{DD}≤5.5V I_{OH1}= -3.0mA	V_{DD}-0.6	-	-	V
			1.8V≤V_{DD}≤5.5V I_{OH1}= -2.0mA	V_{DD}-0.5	-	-	V
	V_{OH2}	PH03~PH04	4.0V≤V_{DD}≤5.5V I_{OH2}= -2.5mA	V_{DD}-1.5	-	-	V
			4.0V≤V_{DD}≤5.5V I_{OH2}= -1.5mA	V_{DD}-0.7	-	-	V
			2.4V≤V_{DD}≤5.5V I_{OH2}= -0.6mA	V_{DD}-0.6	-	-	V
			1.8V≤V_{DD}≤5.5V I_{OH2}= -0.3mA	V_{DD}-0.5	-	-	V
Output voltage, low	V_{OL1}	PA00~PA15, PB00~PB15 PC00~PC14, PD00~PD07 PH00~PH02	4.0V≤V_{DD}≤5.5V I_{OL1}=30.0mA	-	-	1.2	V
			4.0V≤V_{DD}≤5.5V I_{OL1}=15.0mA	-	-	0.7	V
			2.4V≤V_{DD}≤5.5V I_{OL1}=8.0mA	-	-	0.4	V
			1.8V≤V_{DD}≤5.5V I_{OL1}=3.0mA	-	-	0.4	V
	V_{OL2}	PH03~PH04	4.0V≤V_{DD}≤5.5V I_{OL2}=8.0mA	-	-	1.2	V
			4.0V≤V_{DD}≤5.5V I_{OL2}=4.0mA	-	-	0.7	V
			2.4V≤V_{DD}≤5.5V I_{OL2}=2.0mA	-	-	0.4	V
			1.8V≤V_{DD}≤5.5V I_{OL2}=1.0mA	-	-	0.4	V

Remark:

1. Unless otherwise specified, the characteristics of alternate-function pins are the same as the characteristics of the port pins.
2. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Input leakage current, high	I_{LIH1}	PA00~PA15, PB00~PB15 PC00~PC14, PD00~PD07 PH00~PH02	V_I=V_{DD}	-	-	1	uA
	I_{LIH2}	RESETB/PH00	V_I=V_{DD}	-	-	1	uA
	I_{LIH3}	PH03~PH04 (XT1, XT2)	V_I=V_{DD}, when an input port and external clock are inputting	-	-	1	uA
			V_I=V_{DD}, when connecting a resonator	-	-	10	uA
Input leakage current, low	I_{LIL1}	PA00~PA15, PB00~PB15 PC00~PC14, PD00~PD07 PH00~PH02	V_I=V_{SS}	-	-	-1	uA
	I_{LIL2}	RESETB/PH00	V_I=V_{SS}	-	-	-1	uA
	I_{LIL3}	PH03~PH04 (XT1, XT2)	V_I=V_{SS}, when an input port and external clock are inputting	-	-	-1	uA
			V_I=V_{SS}, when connecting a resonator	-	-	-10	uA
Internal pull-up resistance	R_U	PA00~PA15, PB00~PB15 PC00~PC14, PD00~PD07 PH00~PH02	V_I=V_{SS}, when inputting a port	10	30	100	KΩ
Internal pull-down resistance	R_D	PA00~PA15, PB00~PB15 PC00~PC14, PD00~PD07 PH01~PH02	V_I=V_{DD}, when inputting a port	10	30	100	KΩ

Remark:

1. Unless otherwise specified, the characteristics of alternate-function pins are the same as the characteristics of the port pins.
2. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.5.2 Power supply current characteristics

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Run mode	High-speed on-chip oscillator	F_{HOCO}=32MHz, F_{IH}=32MHz Note3		-	3.0	6.5	mA
			High-speed main system clock	F_{MX}=20MHz Note 2	Square wave input	-	3.7	5.0	mA
					Crystal oscillator connection	-	3.7	5.0	
			Subsystem clock operation	F_{SUB}=32.768KHz Note4	Square wave input	-	11.0	85	uA
					Crystal oscillator connection	-	11.0	85	
			Low-speed on-chip oscillator	F_{IL}=32KHz Note8		-	5.1	80	uA
	I_{DD2}	Sleep mode	High-speed on-chip oscillator	F_{HOCO}=32MHz, F_{IH}=32MHz Note3		-	0.9	4.5	mA
			High-speed main system clock	F_{MX}=20MHz Note 2	Square wave input	-	0.7	4.0	mA
					Crystal oscillator connection	-	0.7	4.0	
			Subsystem clock operation	F_{SUB}=32.768KHz Note 5	Square wave input	-	1.85	35	uA
					Crystal oscillator connection	-	1.85	35	
			Low-speed on-chip oscillator	F_{IL}=32KHz Note8		-	1.05	35	uA
	I_{DD3} Note6	Deep sleep mode Note7	T_A= -40℃~25℃ V_{DD}=3.0V			-	0.7	1.2	uA
			T_A= -40℃~85℃ V_{DD}=3.0V			-	0.7	12	
			T_A= -40℃~105℃ V_{DD}=3.0V			-	0.7	20	

Note 1: This is the total current through V_{DD}, including input leakage current fixed to V_{DD} or V_{SS} on the input pin. Typical value: CPU is in multiplication instruction execution (I_{DD1}) and does not include external operating current. Maximum Value: The CPU is in multiply instruction execution (I_{DD1}) and contains external operating current, but does not include current to the A/D converter, LVD circuitry, I/O ports, and internal pull-up or pull-down resistors, nor does it include the current when overwriting the data flash memory.

Note 2: This is when the high-speed on-chip oscillator and the subsystem clock are stopped.

Note 3: This is when the high-speed main and subsystem clock are stopped.

Note 4: This is when the high-speed on-chip oscillator and the high-speed main system clock are stopped.

Note 5: This is when the high-speed on-chip oscillator and the high-speed main system clock are stopped. Contains current to the RTC, but does not include current to 15-bit interval timers and watchdog timers.

Note 6: Current flowing to the RTC, 15-bit interval timer and watchdog timer is not included. The MDSET[1:0] of the LCDM0 register needs to be set to b'11.

Note 7: For current values when the subsystem clock is running in deep sleep mode, refer to current values when the subsystem clock is running in sleep mode.

Note 8: This is when the high-speed on-chip oscillator, the high-speed main system clock and the subsystem clock are stopped.

Remark:

1. F_{HOCO}: High-speed on-chip oscillator clock frequency, F_{IH}: High-speed on-chip oscillator system clock frequency
2. F_{SUB}: External subsystem clock frequency (XT1/ XT2 clock oscillation frequency)
3. F_{MX}: External main system clock frequency (X1/ X2 clock oscillation frequency).
4. F_{IL}: Low-speed on-chip oscillator clock frequency
5. Typical temperature condition: T_A=25℃.
6. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition				Min.	Typ.	Max.	Unit
Low speed on-chip oscillator operating current	I_{FIL} Note 1	-				-	0.2	-	uA
RTC operating current	I_{RTC} Note 1,2,3	-				-	0.04	-	uA
15-bit interval timer operating current	I_{IT} Note 1,2,4	-				-	0.02	-	uA
Watchdog timer operating current	I_{WDT} Note 1,2,5	F_{IL}=32KHz				-	0.22	-	uA
A/D converter operating current	I_{ADC} Note 1,6	ADC HS mode @32MHz				-	2.2	-	mA
		ADC HS mode @4MHz				-	1.3	-	mA
		ADC LC mode @16MHz				-	1.1	-	mA
		ADC LC mode @4MHz				-	0.8	-	mA
OPA operating current		Per channel				-	135	150	uA
CMP operating current	I_{CMP} Note 1,9	Per channel	-			-	60	100	uA
			-			-	80	140	uA
LVD operating current	I_{LVD} Note 1,7	-				-	0.08		uA
LCD operating current	I_{LCD1} Note 1,10,11	External resistance division method	LCD=F_{SUB}	1/3 bias 4 time slices	V_{DD}=5.0V V_{L4}=5.0V	-	0.04	0.2	uA
	I_{LCD2} Note 1,10	Internal voltage boosting method	F_{LCD}=F_{SUB} LCD clock=128 Hz	1/3 bias 4 time slices	V_{DD}=3.0V V_{L4}=3.0V (V_{LCD}=04H)	-	0.85	2.2	uA
					V_{DD}=5.0V V_{L4}=5.1V (V_{LCD}=12H)	-	1.0	4.0	
	I_{LCD3} Note 1,10	Capacitor split method	F_{LCD}=F_{SUB} LCD clock =128Hz	1/3 bias 4 time slices	V_{DD}=3.0V V_{L4}=3.0V	-	0.2	0.5	

Note 1: This is the current flowing through V_{DD}.

Note 2: This is when the high-speed on-chip oscillator and the high-speed system clock are stopped.

Note 3: This is the current that flows only to the real-time clock (RTC) (excluding the operating current of

the low-speed on-chip oscillator and the XT1 oscillation circuit). In the case of a real-time clock operating in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{RTC} value. In addition, I_{FIL} must be added when selecting a low-speed on-chip oscillator. When the subsystem clock is running, I_{DD2} contains the operating current of the real-time clock.

Note 4: This is the current that flows only to the 15-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and XT1 oscillation circuit). In the case of 15-bit interval timer operation in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{IT} value. In addition, I_{FIL} must be added when selecting a low-speed on-chip oscillator.

Note 5: This is the current that flows only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). In the case of watchdog timer operation, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus I_{WDT}.

Note 6: This is the current that only flows to the A/D converter. In the case of A/D converter operation in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{ADC} value.

Note 7: This is the current that only flows to the LVD circuit. In the case of LVD circuit operation, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus the value of I_{LVD}.

Note 8: This is the current that only flows to the D/A converter. In the case of D/A converter operation in run mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the I_{DAC} value.

Note 9: This is the current that only flows to the comparator circuit. In the case of comparator circuit operation, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus the I_{CMP} value.

Note 10: This refers to the current flowing to the LCD controller/driver only. In both operating mode and HALT mode, the current value of the BAT32G127 microcontroller is the power supply current (I_{DD1} or I_{DD2}) plus the LCD operating current (I_{LCD1}, I_{LCD2}, or I_{LCD3}). This does not include the current flowing to the LCD display. Typical and maximum values are based on the following conditions:

- The 20-pin is configured for segment function, with all LEDs on.
- The system clock is set to F_{SUB}, and the LCD clock is 128 Hz (LCDC0=07H).
- Configured with 4 time slices and 1/3 bias.

Note 11: When using an external resistance division method, the current flowing to the external divider resistor is not included.

Remark:

1. F_{IL}: Low-speed on-chip oscillator clock frequency
2. Typical temperature condition: T_A=25℃.
3. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.6 AC characteristics

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Instruction cycle (min instruction execution time)	T_{CY}	Main system clock (F_{MAIN}) operation	1.8V≤V_{DD}≤5.5V	0.03125	-	1	us
		Subsystem clock (F_{SUB}) operation	1.8V≤V_{DD}≤5.5V	28.5	30.5	31.3	us
External system clock frequency	F_{EX}	1.8V≤V_{DD}≤5.5V		1.0	-	20.0	MHz
	F_{EXS}	1.8V≤V_{DD}≤5.5V		32.0	-	35.0	KHz
External system clock input high-level width, low-level width	T_{EXH} T_{EXL}	1.8V≤V_{DD}≤5.5V		24	-	-	ns
	T_{EXHS} T_{EXLS}	1.8V≤V_{DD}≤5.5V		13.7	-	-	us
TI00 ~TI07 inputs high-level width, low-level width	T_{TIH} T_{TIL}	1.8V≤V_{DD}≤5.5V		1/F_{MCK} +10	-	-	ns
TO00 ~ TO07 output frequency	F_{TO}	4.0V≤V_{DD}≤5.5V		-	-	16	MHz
		2.4V≤V_{DD}<4.0V		-	-	8	MHz
		1.8V≤V_{DD}<2.4V		-	-	4	MHz
CLKBUZ0 CLKBUZ1 output frequency	F_{PCL}	4.0V≤V_{DD}≤5.5V		-	-	16	MHz
		2.4V≤V_{DD}<4.0V		-	-	8	MHz
		1.8V≤V_{DD}<2.4V		-	-	4	MHz
Interrupt input high-level width, low-level width	T_{INTH} T_{INTL}	INTP0 ~ INTP5	1.8V≤V_{DD}≤5.5V	1	-	-	us
Key interrupt input high-level width, low-level width	T_{KR}	KR0 ~ KR7	1.8V≤V_{DD}≤5.5V	250	-	-	ns
RESETB low-level width	T_{RSL}	-		10	-	-	us

Remark:

1. F_{MCK}: Timer8 operating clock frequency.
2. Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.7 Peripheral functions characteristics

6.7.1 Universal interface unit

1) UART mode

(T_A= -40~85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Condition		Specification value		Unit
			Min.	Max.	
Transfer rate	1.8V ≤ V_{DD} ≤ 5.5V	-	-	F_{MCK}/6	bps
		Theoretical value of the maximum transfer rate F_{MCK}=F_{CLK}	-	10.6	Mbps

(T_A=85~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Condition		Specification value		Unit
			Min.	Max.	
Transfer rate	1.8V ≤ V_{DD} ≤ 5.5V	-	-	F_{MCK}/12	bps
		Theoretical value of the maximum transfer rate F_{MCK}=F_{CLK}	-	5.3	Mbps

Remark: This specification is guaranteed by the design, and is not tested in mass production.

2) 3-wire SPI mode (master mode, internal clock output)

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		-40 ~ 85℃		85 ~ 105℃		Unit
				Min.	Max.	Min.	Max.	
SCLKp cycle time	T_{KCY1}	T_{KCY1} ⩾ 2/ F_{CLK}	2.7V ⩽ V_{DD} ⩽ 5.5V	62.5	-	125	-	ns
			1.8V ⩽ V_{DD} ⩽ 5.5V	125	-	250	-	ns
SCLKp high/low level width	T_{KH1} T_{KL1}	2.7V ⩽ V_{DD} ⩽ 5.5V		T_{KCY1}/2-5	-	T_{KCY1}/2-10	-	ns
		1.8V ⩽ V_{DD} ⩽ 5.5V		T_{KCY1}/2-19	-	T_{KCY1}/2-38	-	ns
SDIp set-up time (for SCLKp↑)	T_{SIK1}	2.7V ⩽ V_{DD} ⩽ 5.5V		17	-	33	-	ns
		1.8V ⩽ V_{DD} ⩽ 5.5V		28	-	55	-	ns
SDIp hold time (for SCLKp↑)	T_{KSI1}	1.8V ⩽ V_{DD} ⩽ 5.5V		5	-	10	-	ns
Delay time from SCLKp↓→SDOp	T_{KSO1}	1.8V ⩽ V_{DD} ⩽ 5.5V C=20pF Note 1		-	5	-	10	ns

Note 1: C is the load capacitance of the SCLKp, SDOp output lines.

Caution: Through the Port Input Mode Register and Port Output Mode Register, the SDIp pin is selected as the normal input buffer and the SDOp pin and SCLKp pin are selected as the normal output mode.

Remark: This specification is guaranteed by the design, and is not tested in mass production.

3) 3-wire SPI mode (slave mode, external clock input)

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		-40 ~ 85℃		85 ~ 105℃		Unit
				Min.	Max.	Min.	Max.	
SCLKp cycle time	T_{KCY2}	4.0V ≤ V_{DD} ≤ 5.5V	20MHz < F_{MCK}	8/F_{MCK}	-	16/F_{MCK}	-	ns
			F_{MCK} ≤20MHz	6/F_{MCK}	-	12/F_{MCK}	-	ns
		2.7V ≤ V_{DD} ≤ 5.5V	16MHz < F_{MCK}	8/F_{MCK}	-	16/F_{MCK}	-	ns
			F_{MCK} ≤16MHz	6/F_{MCK}	-	12/F_{MCK}	-	ns
		2.4V ≤ V_{DD} ≤ 5.5V		6/F_{MCK} and≥ 500	-	12/F_{MCK} and≥ 1000	-	ns
		1.8V ≤ V_{DD} ≤ 5.5V		6/F_{MCK} and≥ 750	-	12/F_{MCK} and≥ 1500	-	ns
SCLKp high/low level width	T_{KH2} T_{KL2}	4.0V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-7	-	T_{KCY1}/2-14	-	ns
		2.7V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-8	-	T_{KCY1}/2-16	-	ns
		1.8V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-18	-	T_{KCY1}/2-36	-	ns
SDIp set-up time (for SCLKp↑)	T_{SIK2}	2.7V ≤ V_{DD} ≤ 5.5V		1/F_{MCK}+20	-	1/F_{MCK}+40	-	ns
		1.8V ≤ V_{DD} ≤ 5.5V		1/F_{MCK}+30	-	1/F_{MCK}+60	-	ns
SDIp hold time (for SCLKp↑)	T_{KSI2}	1.8V ≤ V_{DD} ≤ 5.5V		1/F_{MCK}+31	-	1/F_{MCK}+62	-	ns
Delay time from SCLKp↓→SDOp	T_{KSO2}	2.7V ≤ V_{DD} ≤ 5.5V C=30pF Note 1		-	2/F_{MCK}+ 44	-	2/F_{MCK}+ 66	ns
		2.4V ≤ V_{DD} ≤ 5.5V C=30pF Note 1		-	2/F_{MCK}+ 75	-	2/F_{MCK}+ 113	ns
		1.8V ≤ V_{DD} ≤ 5.5V C=30pF Note 1		-	2/F_{MCK}+ 100	-	2/F_{MCK}+ 150	ns

Note 1: C is the load capacitance of the SCLKp, SDOp output lines.

Caution: Through the Port Input Mode Register and Port Output Mode Register, the SDIp and SCLKp pins are selected as the normal input buffers and the SDOp pin is selected as the normal output mode.

Remark: This specification is guaranteed by the design, and is not tested in mass production.

4) 4-wire SPI mode (slave mode, external clock input)

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		-40 ~ 85℃		85 ~ 105℃		Unit
				Min.	Max.	Min.	Max.	
SSI00 set-up time	T_{SSIK}	DAPmn= 0	2.7V ≤ V_{DD} ≤ 5.5V	120	-	240	-	ns
			1.8V ≤ V_{DD} ≤ 5.5V	200	-	400	-	ns
		DAPmn= 1	2.7V ≤ V_{DD} ≤ 5.5V	1/F_{MCK}+120	-	1/F_{MCK}+240	-	ns
			1.8V ≤ V_{DD} ≤ 5.5V	1/F_{MCK}+200	-	1/F_{MCK}+400	-	ns
SSI00 hold time	T_{KSSI}	DAPmn= 0	2.7V ≤ V_{DD} ≤ 5.5V	1/F_{MCK}+120	-	1/F_{MCK}+240	-	ns
			1.8V ≤ V_{DD} ≤ 5.5V	1/F_{MCK}+200	-	1/F_{MCK}+400	-	ns
		DAPmn= 1	2.7V ≤ V_{DD} ≤ 5.5V	120	-	240	-	ns
			1.8V ≤ V_{DD} ≤ 5.5V	200	-	400	-	ns

Caution: Select the SDIp and SCLKp pins as the normal input buffers and the SDOp pin as the normal output mode via the Port Input Mode Register and Port Output Mode Register.

Remark: This specification is guaranteed by the design, and is not tested in mass production.

5) Simplified IIC mode

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	-40 ~ 85℃		85 ~ 105℃		Unit
			Min.	Max.	Min.	Max.	
SCLr clock frequency	F_{SCL}	2.7V ≤ V_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ	-	1000Note 1	-	400Note 1	KHz
		1.8V ≤ V_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 kΩ	-	400Note 1	-	100Note 1	KHz
		1.8V ≤ V_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ	-	300Note 1	-	75Note 1	KHz
Hold time when SCLr is low	T_{LOW}	2.7V ≤ V_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ	475	-	1200	-	ns
		1.8V ≤ V_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 kΩ	1150	-	4600	-	ns
		1.8V ≤ V_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ	1550	-	6500	-	ns
Hold time when SCLr is high	T_{HIGH}	2.7V ≤ V_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ	475	-	1200	-	ns
		1.8V ≤ V_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 kΩ	1150	-	4600	-	ns
		1.8V ≤ V_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ	1550	-	6500	-	ns
Data setup time (reception)	$T_{SU:DAT}$	2.7V ≤ V_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ	$1/F_{MCK}$+85Note 2	-	$1/F_{MCK}$+220Note 2	-	ns
		1.8V ≤ V_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 kΩ	$1/F_{MCK}$+145Note 2	-	$1/F_{MCK}$+580Note 2	-	ns
		1.8V ≤ V_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ	$1/F_{MCK}$+230Note 2	-	$1/F_{MCK}$+1200Note 2	-	ns
Data hold time (transmission)	$T_{HD:DAT}$	2.7V ≤ V_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ	-	305	-	770	ns

		1.8V ⩽ V_{DD} ⩽ 5.5V C_b = 100 pF, R_b = 3 kΩ	-	355	-	1420	ns
		1.8V ⩽ V_{DD} ⩽ 2.7V C_b = 100 pF, R_b = 5 kΩ	-	405	-	2070	ns

Note 1: Set the value to F_{MCK}/4.

Note 2: Set the F_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.7.2 Serial interface IICA

1) I^2C standard mode

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLA0 clock frequency	F_{SCL}	Standard mode: F_{CLK}≥1MHz	-	100	KHz
Set-up time of the start condition	$T_{SU: STA}$	-	4.7	-	us
Hold time of the start condition Note1	$T_{HD: STA}$	-	4.0	-	us
Hold time when SCLA0 is low	T_{LOW}	-	4.7	-	us
Hold time when SCLA0 is high	T_{HIGH}	-	4.0	-	us
Data set-up time (reception)	$T_{SU: DAT}$	-	250	-	ns
Data hold time (transmission) Note2	$T_{HD: DAT}$	-	0	3.45	us
Set-up time of the stop condition	$T_{SU: STO}$	-	4.0	-	us
Bus idle time	T_{BUF}	-	4.7	-	us

Note 1: Generate the first clock pulse after a start condition or a restart condition is generated.

Note 2: The maximum value of $T_{HD: DAT}$ needs to be guaranteed during normal transfer and needs to be waited during acknowledger (ACK).

Caution: The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (communication line pull-up resistor value) at this time are as follows:

Standard mode: C_b=400pF, R_b=2.7KΩ

Remark: This specification is guaranteed by the design, and is not tested in mass production.

2) I^2C fast mode

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLA0 clock frequency	F_{SCL}	Fast mode: F_{CLK}≥3.5MHz	-	400	KHz
Set-up time of the start condition	$T_{SU: STA}$	-	0.6	-	us
Hold time of the start condition Note1	$T_{HD: STA}$	-	0.6	-	us
Hold time when SCLA0 is low	T_{LOW}	-	1.3	-	us

Hold time when SCLA0 is high	T_{HIGH}	-	0.6	-	us
Data set-up time (reception)	$T_{SU: DAT}$	-	100	-	ns
Data hold time (transmission) Note2	$T_{HD: DAT}$	-	0	0.9	us
Set-up time of the stop condition	$T_{SU: STO}$	-	0.6	-	us
Bus idle time	T_{BUF}	-	1.3	-	us

Note 1: Generate the first clock pulse after a start condition or a restart condition is generated.

Note 2: The maximum value of $T_{HD: DAT}$ needs to be guaranteed during normal transfer and needs to be waited during acknowledger (ACK).

Caution: The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (pull-up resistor value of the communication line) at this time are as follows:

Fast mode: C_b=320pF, R_b=1.1KΩ

Remark: This specification is guaranteed by the design, and is not tested in mass production.

3) I^2C enhanced fast mode

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLA0 clock frequency	F_{SCL}	Enhanced fast mode: F_{CLK}≥10MHz	-	1000	KHz
Set-up time of the start condition	$T_{SU: STA}$	-	0.26	-	us
Hold time of the start condition Note1	$T_{HD: STA}$	-	0.26	-	us
Hold time when SCLA0 is low	T_{LOW}	-	0.5	-	us
Hold time when SCLA0 is high	T_{HIGH}	-	0.26	-	us
Data set-up time (reception)	$T_{SU: DAT}$	-	50	-	ns
Data hold time (transmission) Note2	$T_{HD: DAT}$	-	0	0.45	us
Set-up time of the stop condition	$T_{SU: STO}$	-	0.26	-	us
Bus idle time	T_{BUF}	-	0.5	-	us

Note 1: Generate the first clock pulse after a start condition or restart condition is generated.

Note 2: The maximum value of $T_{HD: DAT}$ needs to be guaranteed during normal transfer and needs to be waited during acknowledger (ACK).

Caution: The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (pull-up resistor value of the communication line) at this time are as follows:

Enhanced fast mode: C_b=120pF, R_b=1.1KΩ

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.8 Analog characteristics

6.8.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel \ Reference voltage	Reference voltage(+)=AV_{REFP} Reference voltage(–)=AV_{REFM}	Reference voltage(+)=V_{DD} Reference voltage (–)=V_{SS}
ANI0~ANI25	Refer to 6.8.1(1)	Refer to 6.8.1(2)
Internal reference voltage, temperature sensor output voltage		

(1) When selecting reference voltage (+)=AV_{REFP}/ANI0, reference voltage (-)=AV_{REFM}/ANI1

(T_A= -40~105℃, 1.8V≤AV_{REFP}≤V_{DD}≤5.5V, V_{SS}=0V, reference voltage (+)=AV_{REFP}, reference voltage (-)=AV_{REFM}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Resolution	RES	-		-	12	-	bit
Combined error Note 1	AINL	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-	3	-	LSB
Conversion time Note 3	T_{CONV}	12-bit resolution Conversion target: ANI0~ANI25	1.8V≤V_{DD}≤5.5V	45	-	-	T_{MCLK}
		12-bit resolution Conversion target: internal reference voltage, temperature sensor output voltage, OPA output voltage	1.8V≤V_{DD}≤5.5V	72	-	-	T_{MCLK}
Zero scale error Note1	E_{ZS}	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-	0	-	LSB
Full scale error Note1	E_{FS}	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-	0	-	LSB
Integral linearity error Note1	ILE	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-	-	±1	LSB
Differential linearity error Note1	DLE	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-	-	±1.5	LSB
Analog input voltage	V_{AIN}	ANI0~ANI25		0	-	AV_{REFP}	V
		Internal reference voltage (1.8V≤V_{DD}≤5.5V)		V_{BGR} Note 2		V	
		Temperature sensor output voltage (1.8V≤V_{DD}≤5.5V)		V_{TMPS25} Note 2		V	

Note 1: Excludes quantization error (±1/2 LSB).

Note 2: Please refer to 6.8.2 Characteristics of Temperature Sensor/ Internal Reference Voltage.

Note 3: T_{MCLK} is the action clock of the AD, T_{MCLK}=1/F_{ADC}, F_{ADC} is the AD operating frequency, up to 32MHz.

Remark: This specification is guaranteed by the design, and is not tested in mass production.

(2) When selecting reference voltage (+)=V_{DD}, reference voltage (-)=V_{SS}

(T_A= -40~105°C, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V, reference voltage (+)=V_{DD}, reference voltage (-)=V_{SS})

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Resolution	RES	-		-	12	-	bit
Combined error Note 1	AINL	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-	6	-	LSB
Conversion time Note 3	T_{CONV}	12-bit resolution Conversion target: ANI0~ANI25	1.8V≤V_{DD}≤5.5V	45	-	-	T_{MCLK}
		12-bit resolution Conversion target: internal reference voltage, temperature sensor output voltage, OPA output voltage	1.8V≤V_{DD}≤5.5V	72	-	-	T_{MCLK}
Zero scale error Note1	E_{ZS}	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-	0	-	LSB
Full scale error Note1	E_{FS}	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-	0	-	LSB
Integral linearity error Note1	ILE	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-	-	±2	LSB
Differential linearity error Note1	DLE	12-bit resolution	1.8V≤AV_{REFP}≤5.5V	-	-	±3	LSB
Analog input voltage	V_{AIN}	ANI0~ANI25		0	-	V_{DD}	V
		Internal reference voltage (1.8V≤V_{DD}≤5.5V)		V_{BGR} Note 2		V	
		Temperature sensor output voltage (1.8V≤V_{DD}≤5.5V)		V_{TMPS25} Note 2		V	

Note 1: Excludes quantization error (±1/2 LSB).

Note 2: Please refer to 6.8.2 Characteristics of Temperature Sensor/ Internal Reference Voltage.

Note 3: T_{MCLK} is the action clock of the AD, T_{MCLK}=1/F_{ADC}, F_{ADC} is the AD operating frequency, up to 32MHz.

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.8.2 Characteristics of temperature sensor/internal reference voltage

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Temperature sensor output voltage	V_{TMPS25}	ADS register=80H, T_A=25℃	-	1.09	-	V
Internal reference voltage	V_{BGR}	ADS register=81H	1.38Note 1	1.45	1.5Note 1	V
Temperature coefficient	F_{VTMPS}	-	-	-3.5	-	mV/℃
Operation stabilization wait time	T_{AMP}	-	5	-	-	us

Remark: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.8.3 Comparator

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Input offset voltage	V_{IOCMP}	-		-	±10	±40	mV
Input voltage range	I_{VCMP}	-		0	-	V_{DD}	V
Internal reference voltage offset	ΔV_{IREF}	CmRVM register: 7FH ~ 80H (m = 0, 1)		-	-	±2	LSB
		Others		-	-	±1	LSB
Response time	T_{CR}, T_{CF}	Input amplitude±100mV		-	70	150	ns
Operation stability time Note1	T_{CMP}	CMPn=0->1	V_{DD}= 3.3 ~ 5.5V	-	-	1	us
			V_{DD}= 1.8 ~ 3.3V	-	-	3	
Reference voltage stabilization time	T_{VR}	CVRE=0->1Note 2		-	-	20	us
Operating current	I_{CMPDD}	Refer to 6.5.2 Power supply current characteristics					

Note 1: The time required from the comparator action enable (CMPnEN=0 ->1) to fulfill each DC/AC style requirement of the CMP.

Note 2: After the internal reference voltage generator is enabled (by setting the CVREm bit to 1; m = 0 to 1), the comparator output can be enabled only after the reference voltage stabilization time has elapsed (CnOE bit = 1; n = 0 to 1).

Remark: Low-temperature specification values are guaranteed by the design, and are not tested in mass production.

6.8.4 Operational Amplifier (OPA)

OPA electrical characteristics

T_A＝25℃, V_{DD}＝5V, unless otherwise specified.

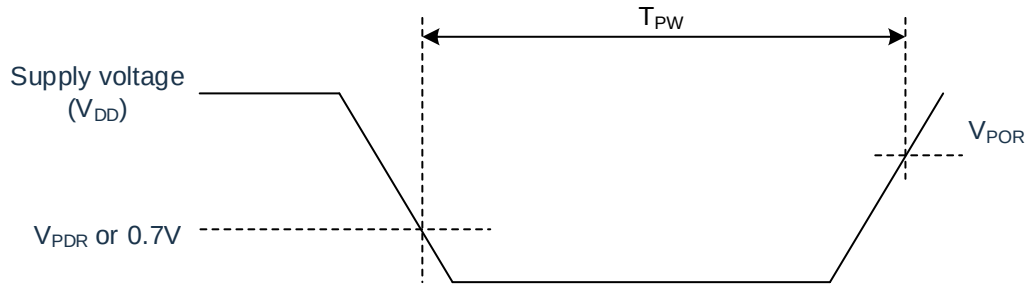
Symbol	Item	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	-	2.5	-	5.5	V
I_Q	Quiescent current	V_{OUT}=2V	-	0.5	0.8	mA
I_{SD}	Shutdown current	-	-	10	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input characteristics						
V_{OS}	Input offset voltage	buffer mode, V_{IN+}=2.5V	-8	-	8	mV
V_{CM}	Common mode input voltage range	-	0.1	-	V_{DD}-0.1	V
I_B	Input bias current	-	-	10	-	pA
Output characteristics						
C_{LOAD}	Capacitive load	-	-	10	-	pF
V_{OH}	Maximum output voltage	I_{LOAD}=0.1mA I_{LOAD}=1mA	- -	- -	V_{DD}-0.1 V_{DD}-0.3	V
V_{OL}	Minimum output voltage	I_{LOAD}=0.1mA I_{LOAD}=1mA	0.1 0.3	- -	- -	V
Frequency characteristics						
A_{OL}	Open loop gain	C_{LOAD}=10pF, buffer mode	-	80	-	dB
BW	Band width	C_{LOAD}=10pF, buffer mode	-	5	-	MHz
PSRR	Power supply rejection ratio	-	-	-80	-	dB
CMRR	Common mode rejection ratio	-40℃~105℃	-	-80	-	dB
Transient characteristics						
SR	Slew rate	C_{LOAD}=10pF, buffer mode	-	8	-	V/us
T_{STB}	Stabilization time	-	-	-	2	us

6.8.5 POR circuit characteristics

(T_A= -40~105℃, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detect voltage	V_{POR}	When the supply voltage rises	-	1.50	1.75	V
	V_{PDR}	When the supply voltage drops	1.37	1.45	1.53	V
Minimum pulse width Note1	T_{PW}	-	300	-	-	us

Note 1: This is the time required to reset the POR when V_{DD} falls below V_{PDR}. In addition, when the oscillation of the main system clock (F_{MAIN}) is stopped by setting bit0 (HIOSTOP) and bit7 (MSTOP) of the clock operation status control register (CSC) in the deep sleep mode, this is the time required for POR reset from the time when V_{DD} is lower than 0.7V to the time when it rises above V_{POR}.



Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.8.6 LVD circuit characteristics

1) Reset mode, interrupt mode

(T_A= -40~105℃, V_{PDR}≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection voltage	V_{LVD0}	When the supply voltage rises	-	4.06	4.26	V
		When the supply voltage drops	3.78	3.98	-	V
	V_{LVD1}	When the supply voltage rises	-	3.75	-	V
		When the supply voltage drops	-	3.67	-	V
	V_{LVD2}	When the supply voltage rises	-	3.13	-	V
		When the supply voltage drops	-	3.06	-	V
	V_{LVD3}	When the supply voltage rises	-	3.02	-	V
		When the supply voltage drops	-	2.96	-	V
	V_{LVD4}	When the supply voltage rises	-	2.92	-	V
		When the supply voltage drops	-	2.86	-	V
	V_{LVD5}	When the supply voltage rises	-	2.81	-	V
		When the supply voltage drops	-	2.75	-	V
	V_{LVD6}	When the supply voltage rises	-	2.71	-	V
		When the supply voltage drops	-	2.65	-	V
	V_{LVD7}	When the supply voltage rises	-	2.61	-	V
		When the supply voltage drops	-	2.55	-	V
	V_{LVD8}	When the supply voltage rises	-	2.50	-	V
		When the supply voltage drops	-	2.45	-	V
	V_{LVD9}	When the supply voltage rises	-	2.09	-	V
		When the supply voltage drops	-	2.04	-	V
	V_{LVD10}	When the supply voltage rises	-	1.98	-	V
		When the supply voltage drops	-	1.94	-	V
	V_{LVD11}	When the supply voltage rises	-	1.88	1.97	V
		When the supply voltage drops	1.75	1.84	-	V
Minimum pulse width	T_{LW}	-	300	-	-	us
Detection delay	-	-	-	-	300	us

Remark: This specification is guaranteed by the design, and is not tested in mass production.

2) Interrupt & reset mode

(T_A= -40~105℃, $V_{PDR} \leqslant V_{DD} \leqslant 5.5V$, V_{SS}=0V)

Item	Symbol	Condition			Min.	Typ.	Max.	Unit
Interrupt & reset mode	V_{LVDB0}	V_{POC2}=0 V_{POC1}=0 V_{POC0}=1	Falling reset voltage		1.78	1.84	-	V
	V_{LVDB1}		LVIS1=1 LVIS0=0	Rising release reset voltage	-	1.98	2.04	V
				Falling interrupt voltage	1.88	1.94	-	V
	V_{LVDB2}		LVIS1=0 LVIS0=1	Rising release reset voltage	-	2.09	-	V
				Falling interrupt voltage	-	2.04	-	V
	V_{LVDB3}		LVIS1=0 LVIS0=0	Rising release reset voltage	-	3.13	-	V
				Falling interrupt voltage	-	3.06	-	V
	V_{LVDC0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=0	Falling reset voltage		-	2.45	-	V
	V_{LVDC1}		LVIS1=1 LVIS0=0	Rising release reset voltage	-	2.61	-	V
				Falling interrupt voltage	-	2.55	-	V
	V_{LVDC2}		LVIS1=0 LVIS0=1	Rising release reset voltage	-	2.71	-	V
				Falling interrupt voltage	-	2.65	-	V
	V_{LVDC3}		LVIS1=0 LVIS0=0	Rising release reset voltage	-	3.75	-	V
				Falling interrupt voltage	-	3.67	-	V
	V_{LVDD0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=1	Falling reset voltage		-	2.75	-	V
	V_{LVDD1}		LVIS1=1 LVIS0=0	Rising release reset voltage	-	2.92	-	V
				Falling interrupt voltage	-	2.86	-	V
	V_{LVDD2}		LVIS1=0 LVIS0=1	Rising release reset voltage	-	3.02	-	V
				Falling interrupt voltage	-	2.96	-	V
	V_{LVDD3}		LVIS1=0 LVIS0=0	Rising release reset voltage	-	4.06	4.26	V
				Falling interrupt voltage	3.78	3.98	-	V

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.8.7 Rising slope characteristics of supply voltage

(T_A= -40~105℃, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Rising slope of supply voltage	SV_{DD}	-	-	-	54	V/ms

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.8.8 LCD characteristics

6.8.8.3 Resistance division method

1) Static mode

(T_A= -40~105℃, V_{L4}(Min.)≤V_{DD}=EV_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L4}	-	2	-	V_{DD}	V

2) 1/2 bias, 1/4 bias

(T_A= -40~105℃, V_{L4}(Min.)≤V_{DD}=EV_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L4}	-	2.7	-	V_{DD}	V

3) 1/3 bias

(T_A= -40~105℃, V_{L4}(Min.)≤V_{DD}=EV_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L4}	-	2.5	-	V_{DD}	V

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.8.8.4 Internal voltage boosting method

(1) 1/3 bias

(T_A= -40~105℃, 1.8V≤V_{DD}=EV_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Variable range of LCD output voltage	V_{L1}	C1~C4[Note 1]=0.47uF[Note 2]	V_{LCD}=03H	0.90	1.00	1.08	V
			V_{LCD}=04H	0.95	1.05	1.13	V
			V_{LCD}=05H	1.00	1.10	1.18	V
			V_{LCD}=06H	1.05	1.15	1.23	V
			V_{LCD}=07H	1.10	1.20	1.28	V
			V_{LCD}=08H	1.15	1.25	1.33	V
			V_{LCD}=09H	1.20	1.30	1.38	V
			V_{LCD}=0AH	1.25	1.35	1.43	V
			V_{LCD}=0BH	1.30	1.40	1.48	V
			V_{LCD}=0CH	1.35	1.45	1.53	V
			V_{LCD}=0DH	1.40	1.50	1.58	V
			V_{LCD}=0EH	1.45	1.55	1.63	V
			V_{LCD}=0FH	1.50	1.60	1.68	V
			V_{LCD}=10H	1.55	1.65	1.73	V
			V_{LCD}=11H	1.60	1.70	1.78	V
			V_{LCD}=12H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1~C4[Note 1]=0.47uF[Note 2]		$2V_{L1}$-0.10	$2V_{L1}$	$2V_{L1}$	V
Tripler output voltage	V_{L4}	C1~C4[Note 1]=0.47uF[Note 2]		$3V_{L1}$-0.15	$3V_{L1}$	$3V_{L1}$	V
Set-up time of reference voltage[Note 2]	T_{VWAIT1}	-		5.00	-	-	ms
Voltage boost wait time[Note 3]	T_{VWAIT2}	C1~C4[Note 1]=0.47uF[Note 2]		500.00	-	-	ms

Note 1: This A capacitor connected between the LCD and the drive voltage pin.

C1: A capacitor connected between CAPH and CAPL.

C2: A capacitor connected between VL1 and GND.

C3: A capacitor connected between VL2 and GND.

C4: A capacitor connected between VL4 and GND.

C1=C2=C3=C4=0.47uF±30%

Note 2: This is the wait time from when the reference voltage is set via the VLCD register (when the reference voltage is used at the default value, it is selected as the internal voltage boosting method (The MDSET1 and MDSET0 of the LCDM0 register=01B)) to when the boost is started (VLCON=1).

Note 3: This is the wait time from the start of boosting (VLCON=1) until the display is enabled (LCDON=1).

Remark: This specification is guaranteed by the design, and is not tested in mass production.

(2) 1/4 bias

(T_A= -40~105℃, 1.8V≤V_{DD}=EV_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Variable range of LCD output voltage	V_{L1}	C1~C5[Note 1]=0.47uF[Note 2]	V_{LCD}=03H	0.90	1.00	1.08	V
			V_{LCD}=04H	0.95	1.05	1.13	V
			V_{LCD}=05H	1.00	1.10	1.18	V
			V_{LCD}=06H	1.10	1.15	1.23	V
			V_{LCD}=07H	1.05	1.20	1.28	V
			V_{LCD}=08H	1.10	1.25	1.33	V
			V_{LCD}=09H	1.20	1.30	1.38	V
Doubler output voltage	V_{L2}	C1~C5[Note 1]=0.47uF[Note 2]		$2V_{L1}$-0.08	$2V_{L1}$	$2V_{L1}$	V
Tripler output voltage	V_{L3}	C1~C5[Note 1]=0.47uF[Note 2]		$3V_{L1}$-0.12	$3V_{L1}$	$3V_{L1}$	V
Quadruply output voltage	V_{L4}	C1~C5[Note 1]=0.47uF[Note 2]		$3V_{L1}$-0.16	$4V_{L1}$	$4V_{L1}$	V
Set-up time of reference voltage[Note 2]	T_{VWAIT1}	-		5.00	-	-	ms
Voltage boost wait time[Note 3]	T_{VWAIT2}	C1~C5[Note 1]=0.47uF[Note 2]		500.00	-	-	ms

Note 1: This A capacitor connected between the LCD and the drive voltage pin.

C1: A capacitor connected between CAPH and CAPL.

C2: A capacitor connected between VL1 and GND.

C3: A capacitor connected between VL2 and GND.

C4: A capacitor connected between VL3 and GND.

C5: A capacitor connected between VL4 and GND.

C1=C2=C3=C4=C5=0.47uF±30%

Note 2: This is the wait time from when the reference voltage is set via the VLCD register (when the reference voltage is used at the default value, it is selected as the internal voltage boosting method (The MDSET1 and MDSET0 of the LCDM0 register=01B)) to when the boost is started (VLCON=1).

Note 3: This is the wait time from the start of boosting (VLCON=1) until the display is enabled (LCDON=1).

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.8.8.5 Capacitor split method

(1) 1/3 bias

(T_A= -40~105℃, 2.2V≤V_{DD}=EV_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{L4} voltage	V_{L4}	C1~C4[Note 1]=0.47uF[Note 2]	-	V_{DD}	-	V
V_{L2} voltage	V_{L2}	C1~C4[Note 1]=0.47uF[Note 2]	2/3V_{L4}-0.1	2/3V_{L4}	2/3V_{L4}+0.07	V
V_{L1} voltage	V_{L1}	C1~C4[Note 1]=0.47uF[Note 2]	1/3V_{L4}-0.08	1/3V_{L4}	1/3V_{L4}+0.08	V
Capacitor split wait time[Note 1]	T_{WAIT}	-	100.00	-	-	ms

Note 1: This is the wait time from the start of boosting (VLCON=1) until the display is enabled (LCDON=1).

Note 2: This A capacitor connected between the LCD and the drive voltage pin.

C1: A capacitor connected between CAPH and CAPL.

C2: A capacitor connected between VL1 and GND.

C3: A capacitor connected between VL2 and GND.

C4: A capacitor connected between VL4 and GND.

C1=C2=C3=C4=0.47uF±30%

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.9 Memory characteristics

6.9.1 Flash memory

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Symbol	Item	Test condition	Min.	Max.	Unit
T_{PROG}	Word program (32bit)	T_A= -40~105℃	24	30	us
T_{ERASE}	Sector erase (512B)	T_A= -40~105℃	4	5	ms
	Chip erase	T_A= -40~105℃	20	40	ms
N_{END}	Endurance	T_A= -40~105℃	100	-	Kcycles
T_{RET}	Data retention	100Kcycles(Note 1) at T_A = 105℃	20	-	Years

Note 1: Cycling performed over the whole temperature range.

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.9.2 RAM memory

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Symbol	Item	Test condition	Min.	Max.	Unit
$V_{RAMHOLD}$	RAM hold vltage	T_A= -40~105℃	0.8	-	V

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.10 EMS characteristics

6.10.1 ESD eletrical characteristics

Symbol	Item	Test condition	Grade
$V_{ESD(HBM)}$	Electrostatic discharge (Human-Body Model HBM)	T_A = 25°C conforming to JESD22-A114	3A

Remark: This specification is guaranteed by the design, and is not tested in mass production.

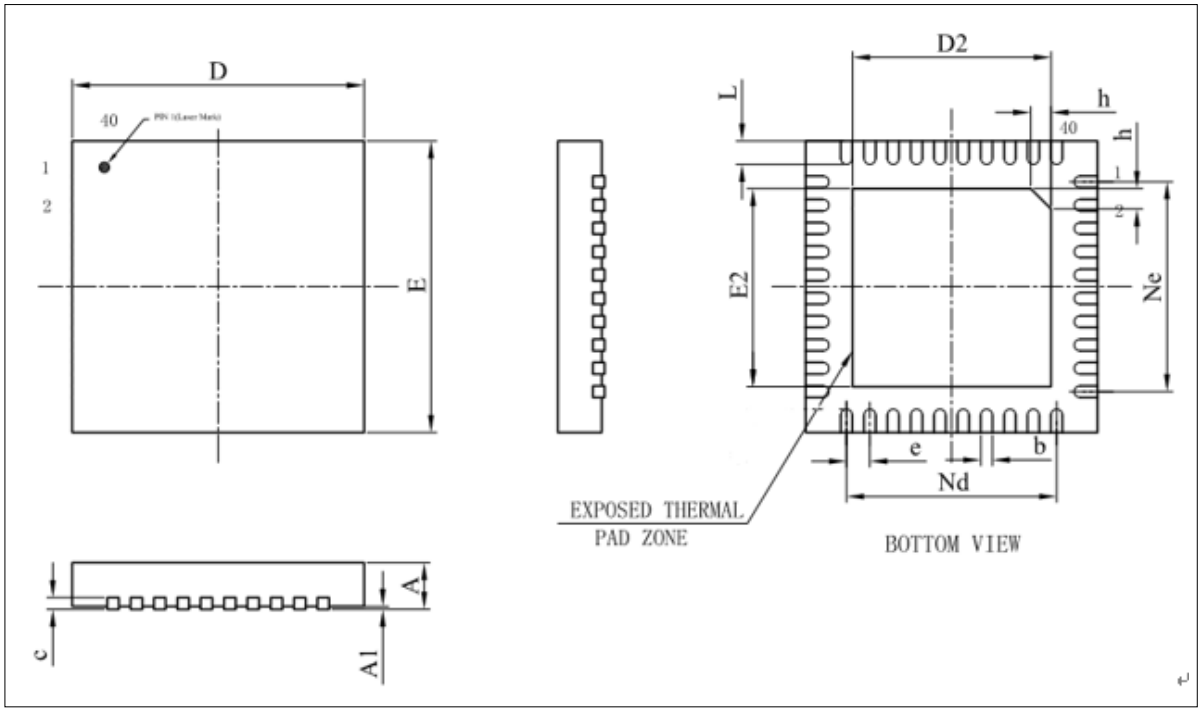
6.10.2 Latch-up electrical characteristics

Symbol	Item	Test condition	Classification
LU	Static latch-up class	T_A = 25°C, conforming to JESD78F	I level B

Remark: This specification is guaranteed by the design, and is not tested in mass production.

7 Package Dimensions

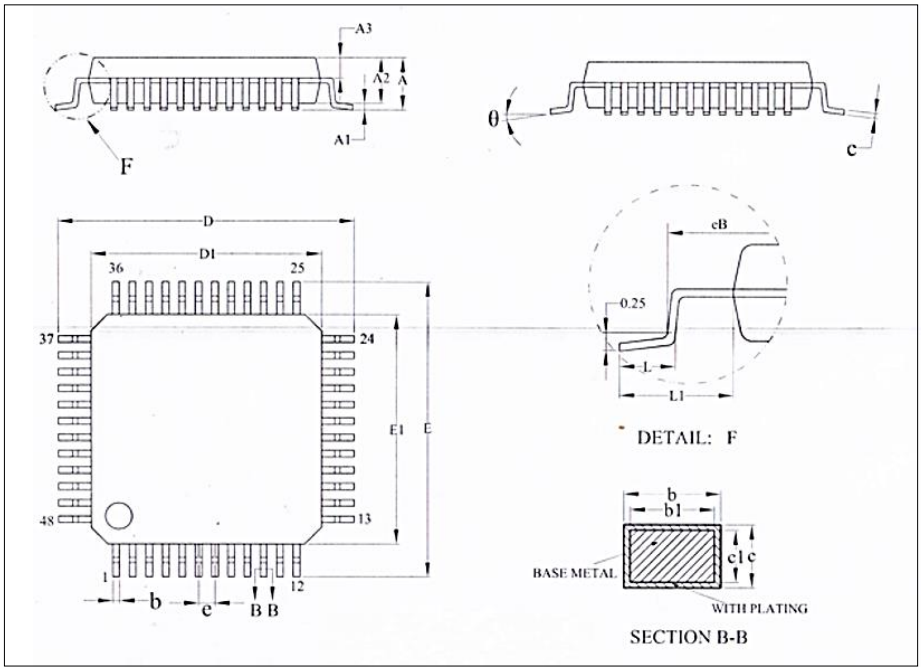
7.1 QFN40 (5x5mm, 0.4mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	-	3.80
e	0.40BSC		
Ne	3.60BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	-	3.80
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

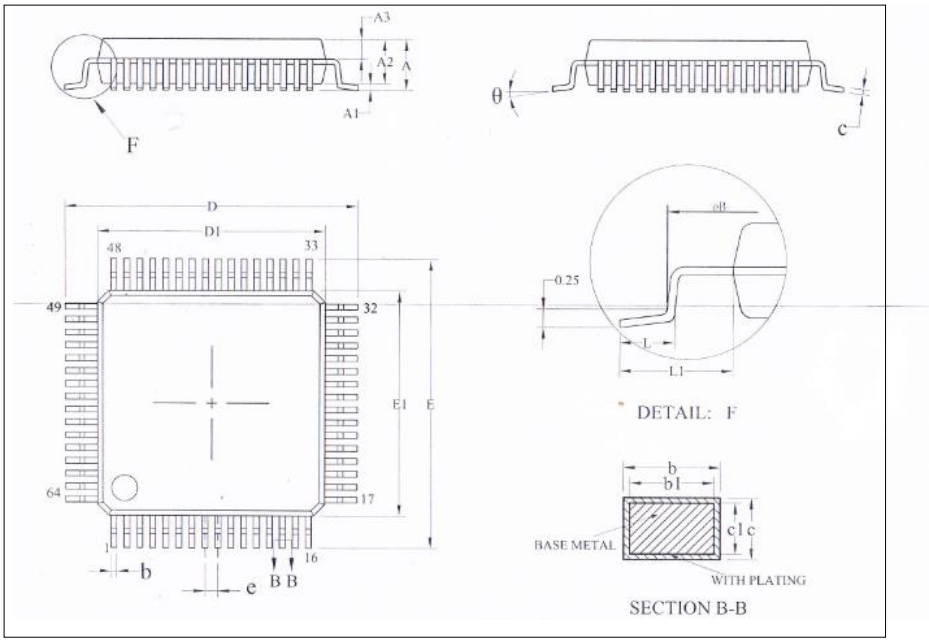
7.2 LQFP48 (7x7mm, 0.5mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.43	-	0.75
L1	1.00REF		
θ	0°	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

7.3 LQFP64 (7x7, 0.4mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	-	0.24
b1	0.15	0.18	0.21
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.40BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

Caution: Package dimensions do not include mold flash or gate burrs.

8 Revision History

Version	Date	Description of changes
V0.1.0	August 2022	Initial version
V0.1.1	February 2023	1) Corrected descriptions in Section 1.2 2) Updated the pin map in Section 1.3.1
V0.1.2	March 2023	1) Updated the pin map in Section 1.3.2 2) Modified the deep sleep mode parameters 3) Updated the format 4) Modified low-speed on-chip oscillator clock frequency values
V0.1.3	August 2023	1) Optimized 1.1 Brief introduction 2) Modified the ADC conversion rate in Section 5.21 3) Modified 6.1 Typical application peripheral circuit
V0.1.4	September 2023	1) Updated 6.1 Typical application peripheral circuit 2) Adjusted the pin map format
V0.1.5	November 2023	1) Deleted related model and contents of the LQFP32 package. 2) Modified the low-speed on-chip oscillator clock frequency value.
V0.1.6	March 2024	1) Updated the pin map in Section 1.3.2 2) Updated data in Sections 6.4.2 and 6.5.2 3) Modified Section 6.1 Typical application peripheral circuit 4) Modified the XT1 clock oscillator capacitor values in section 6.1/6.4.1
V0.1.7	July 2024	Modified package dimensions for QFN40/LQFP48
V0.1.8	September 2024	1) Revised the cover page 2) Modify the Latch_up test standard 3) Correct 1.1 Brief introduction